

662T-M

Rev: 1.2

Page Index =====

Revision History :

Ver A: 1. First Realse

- Ver 1.0:
1. Remove RTL8201CL Co-lay
 2. Change PWM Spec
 3. Single Fuse For Each USB Port
 4. Add SLP_S5- Signal For DIMM Power Control
 5. FIX GLED GPIO Selection To GPIO14
 6. Reverse GPIO 11 For Lan-Phy AC131 Reset
 7. Modify DIMM SPD Power BY VCC3
 8. Change LAN ESD Part From BAV99 to SRV05
 9. Modify ICSPR600 Vttpwr GD By ISL6312 PWGD and Spilit NB TESTMODE2 Circuit
 10. Modify 3-Pin Fan Control Transistor To TO-251

Ver 1.1: For 662 FSB OC 1066 MHz

Ver 1.1A PCB : 15-Q73-011110

Ver 1.1A BOM : 89-206-Q73130 For 662 FSB 1066 MHz

Ver 1.1A BOM : 81-605-Q73131 For 662 FSB 800 MHz

Ver 1.1A BOM : 81-605-Q73132 For 662 OC 1066 MHz

Ver 1.2 PCB : 15-Q73-011200

Ver 1.2 BOM : 89-386-Q73140 For 662 FSB 1066 MHz


Ver 1.2 BOM : 89-386-Q73141 For 662 FSB 800 MHz


Ver 1.2 BOM : 89-206-Q73142 For 662 OC 1066 MHz

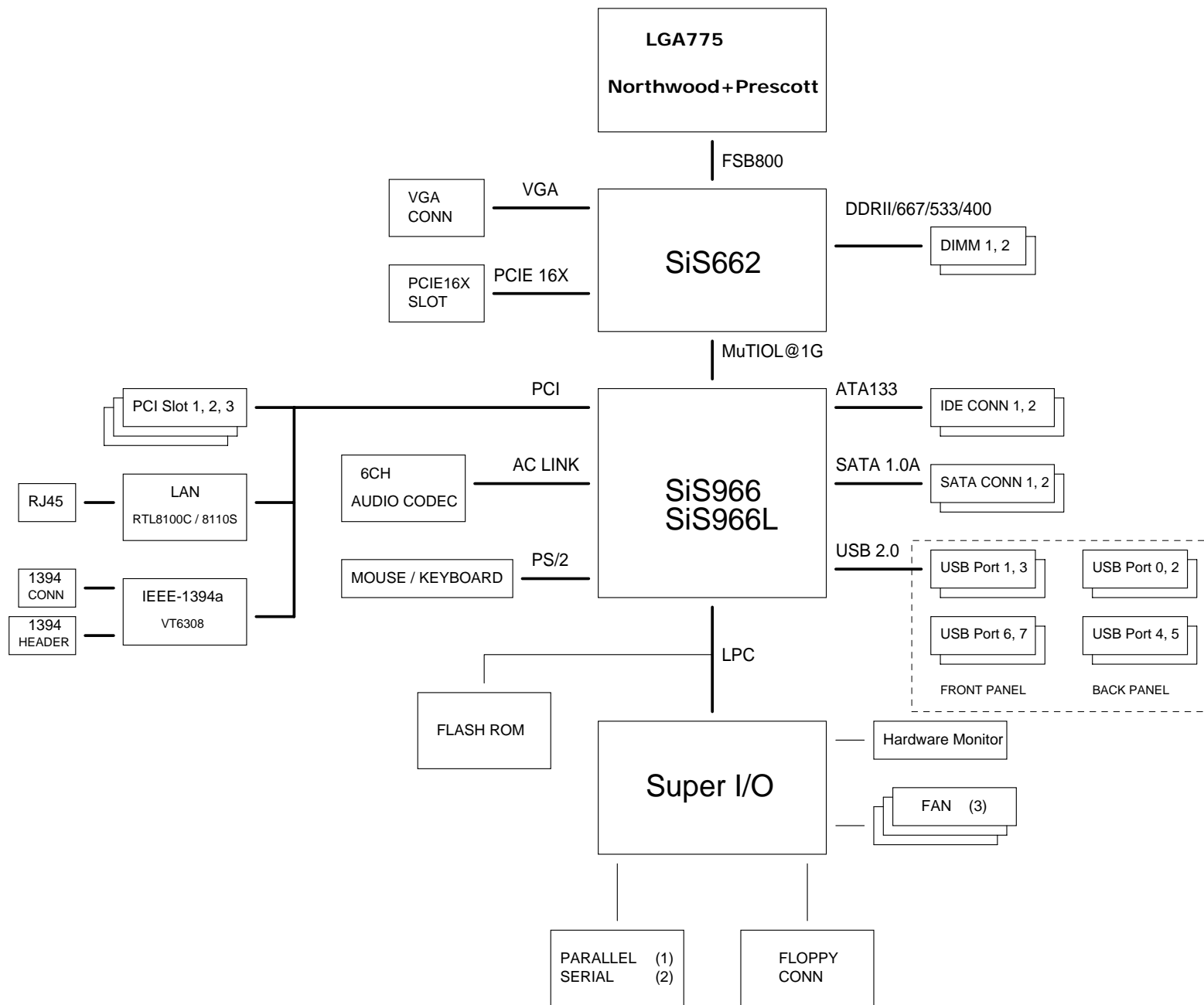
1. Cover Sheet
2. Block Diagram
3. Clock & Power Distribution
4. Socket LGA775-1
5. Socket LGA775-2
6. Socket LGA775-3
7. SiS649-1 (HOST / PCI-EX)
8. SiS649-2 (Memory)
9. SiS649-3 (LINK)
10. SiS649-4 (Power)
11. SiS965-1 (PCI / IDE / HyperZip)
12. SiS965-2 (Misc. Signals)
13. SiS965-3 (USB)
14. SiS965-4 (Power)
15. Main Clock
16. Clock Buffer
17. DDR DIMMII 1, 2
18. DDRII Termination
19. PCI-EXPRESS *16
20. VGA / IDE Connectors
21. USB Connector
22. PCI Slot1, 2
23. PCI3 / LANPHY
24. PCILAN
25. IEEE1394a
26. Audio Codec
27. Audio Interface
28. Super I/O
29. KB/MS/ROM/FDC/IR
30. COM 1,2 / LPT
31. HM/FAN/RING/LPC
32. Voltage Regulator
33. DUAL 5V, 3V& SB Regulator
34. VRD10 (CPU Vcore)
35. ATX / Panel / RTC
36. BOM and GPIO Attention

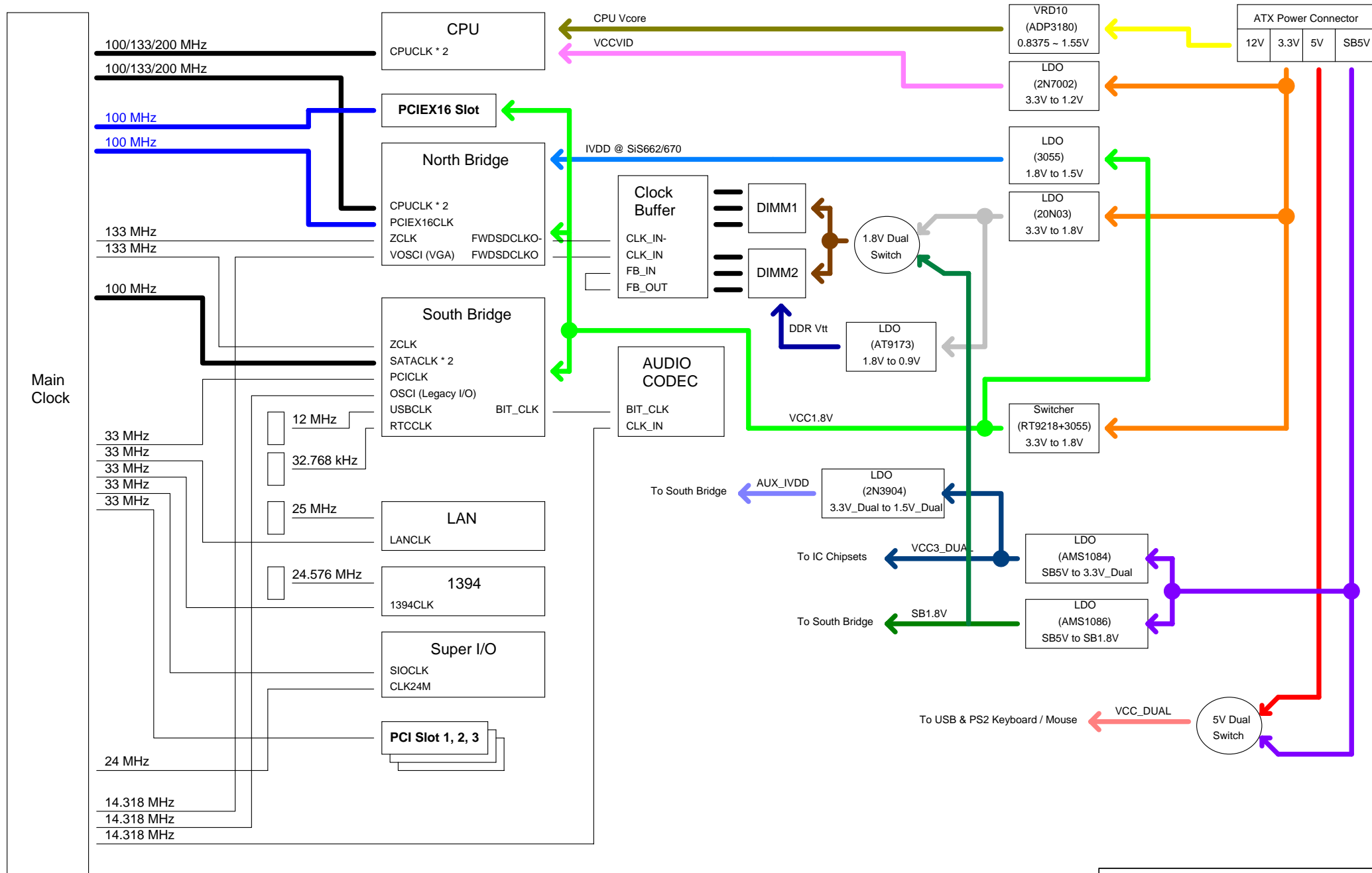
Update note:

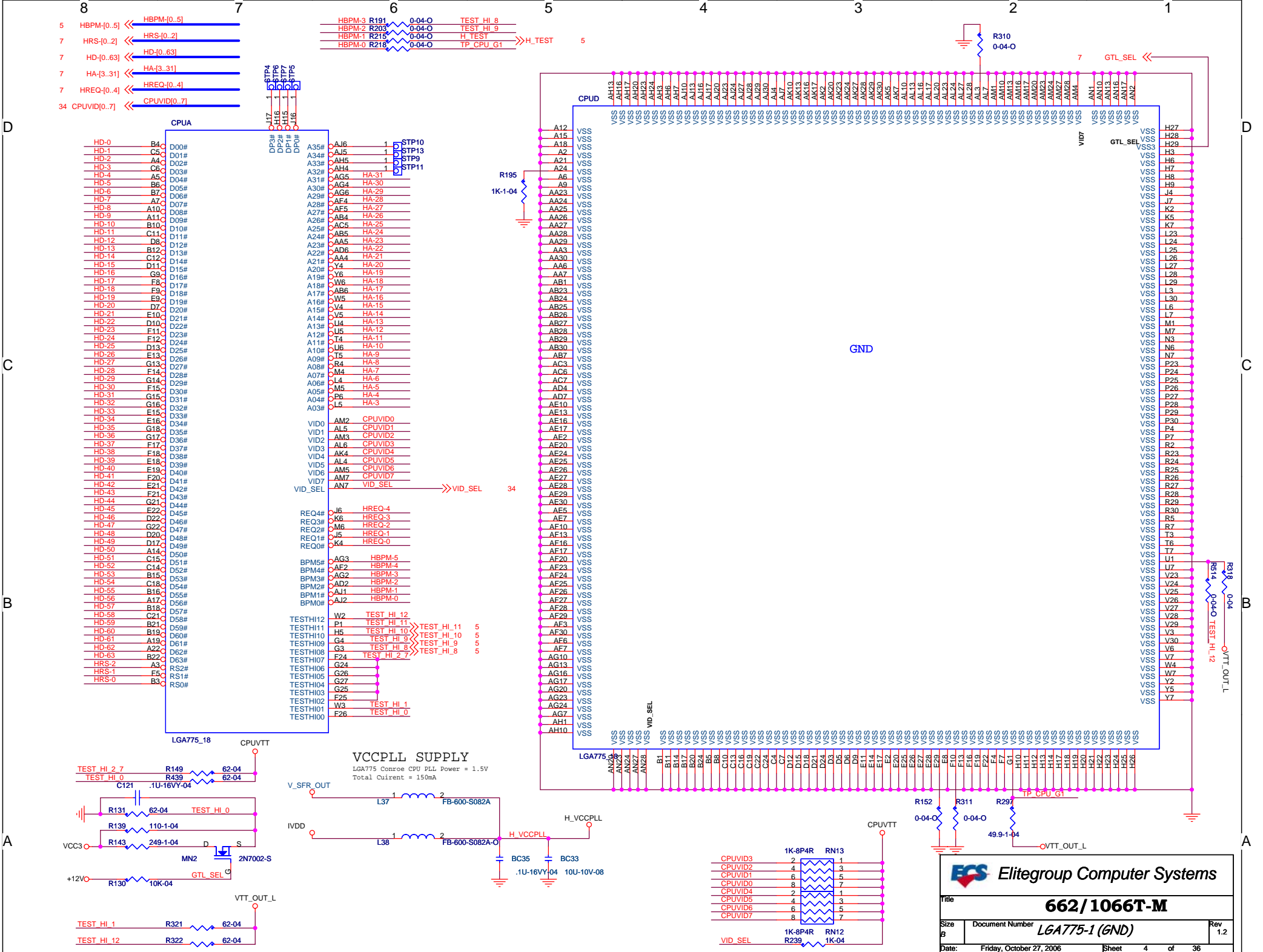
1. Page 5, modified R162 from 100 to 49.9.
2. Page 7, modified R126 from 14 to 10.
. Page 7, modified R117 from 100 to 120.
. Page 7, modified R756 from 619 to 261.
. Page 7, modified SR1 from 100 to 49.9.
. Page 7, modified SR4 from 169 to 100.
3. Page 15, modified R840, R841, and R842 from 1K to 4.7K.
and R843, R844, and R845 from 4.7K to 1K.
4. Page7, modified R804 from 124 to 150.
5. Page7, modified R805 from 500 to 680.
6. Page 34, modified PWM.
7. Page 8, R810 pull high to Vcc3.
8. Page 12, delete 965 KB/MS controller.
. Page 12, modified R873, R874 from 1K to 4.7K.
9. Page 15, modified R73 from 22 to 33.
10. Page 15, modified C68 from 10p to 22p.
. Page 15, modified C101 from 10p to 22p.
11. Page 21, add U26-U29 four ESD IC.
. Page 21, add C1014 and C1016 for EMI.
12. Page 24, add D705-D708 four surge IC.
13. Page 26, add D703 and D704 for preventing pop noise.
14. Page 27, add C1018, C1019, and C1020 for EMI.
15. Page 27, add C1012(1U) to solve MIC issue.
16. Page 27, fine tune audio interface resistance and capacitance.
17. Page 28, changed ITE 8705 to ITE 8712.
18. Page 32, modified R288 from 200 to 187.
19. Page 33, use Q7 and Q8 to replace Vcc_Dual circuit.
20. Page 5, modified to support Smithfield.
21. Page 7, Add Q15,R257 (06.09.20)

	SIGNATURE	DATE
DESIGNER	<i>Jason</i>	
LAYOUT	<i>ECS Layout team</i>	
CHECK	<i>Jason</i>	
APPROVAL		

 Elitegroup Computer Systems		
File 662/1066T-M		
Size Custom	Document Number Cover Sheet	Rev 1.2
Date: Friday, October 27, 2006	Sheet 1	of 36

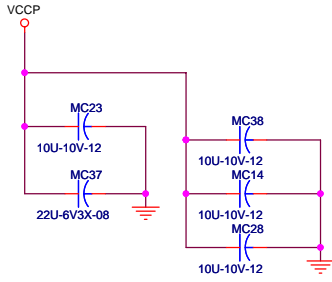




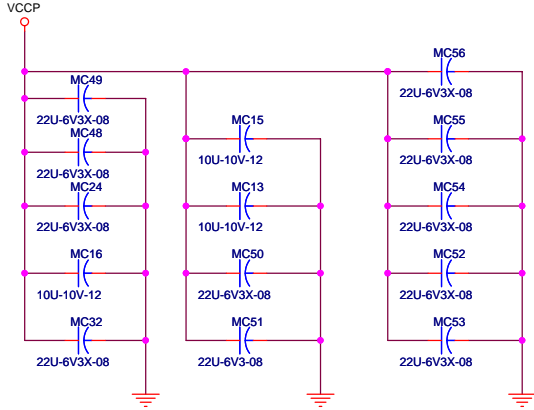


P.S. Choose X5R components instead of Y5V for all 22uF_1206 capacitors on this page.

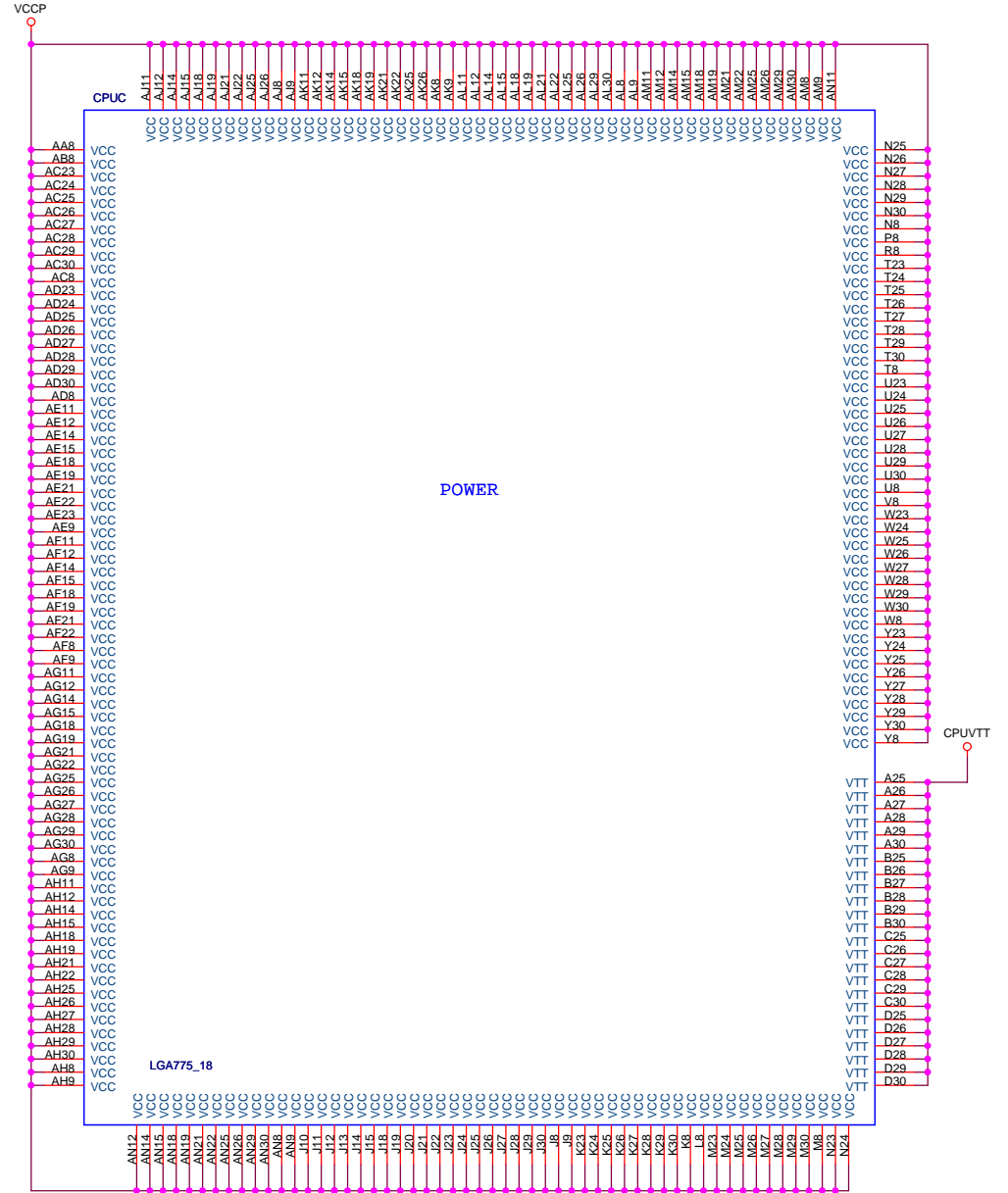
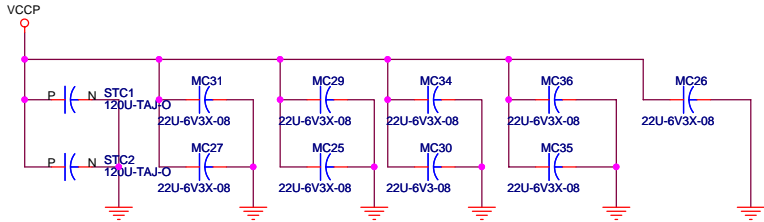
Put these capacitors at processor TOP SIDE



Put these capacitors at processor LEFT SIDE



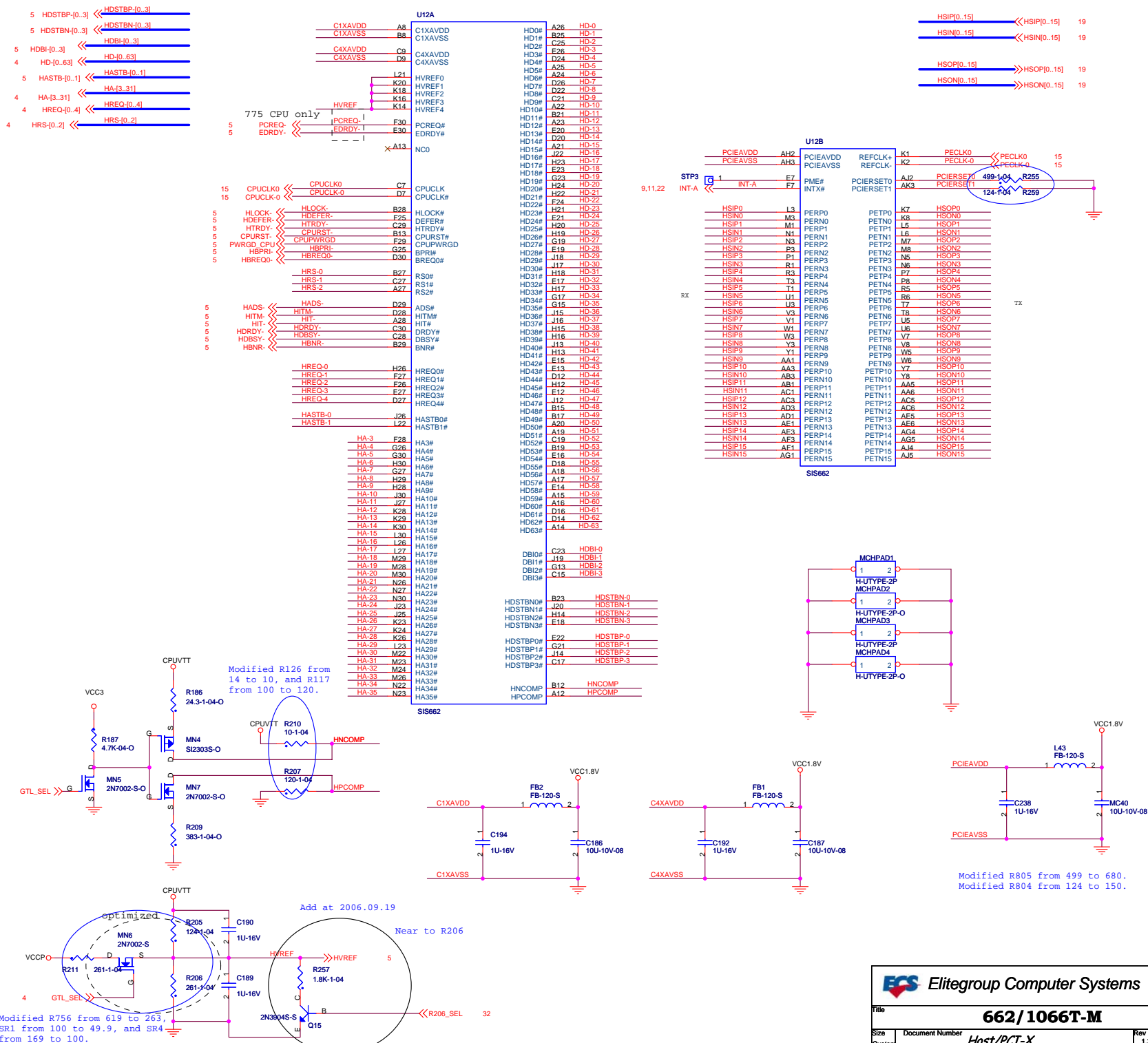
Put these capacitors INSIDE PROCESSOR CAVITY

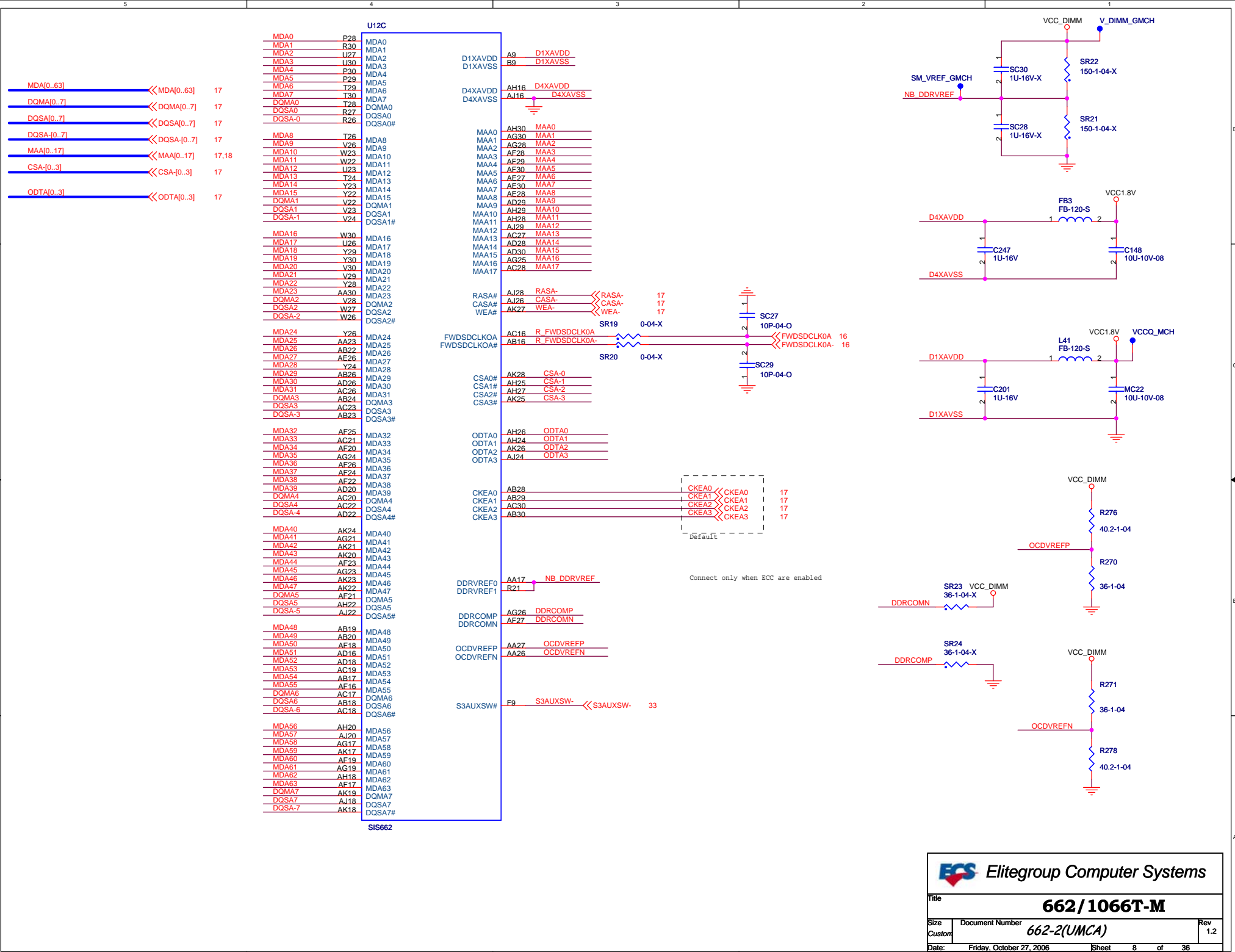


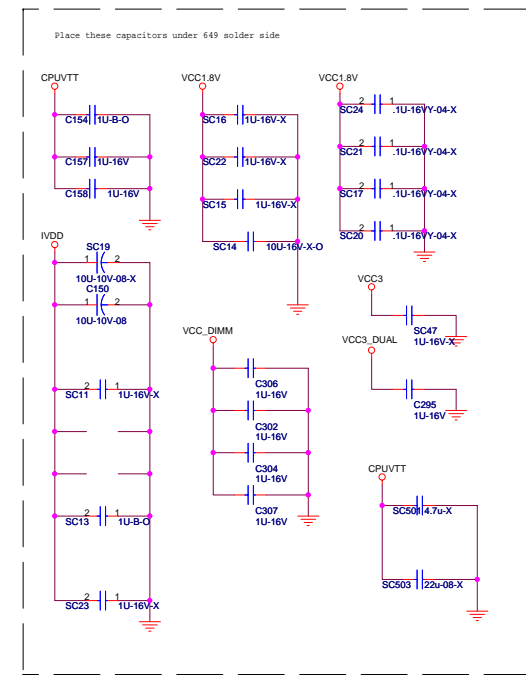
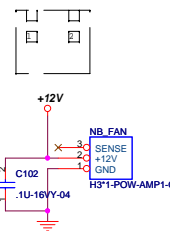
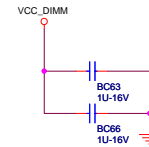
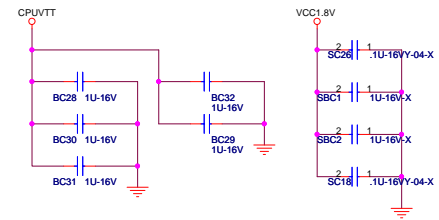
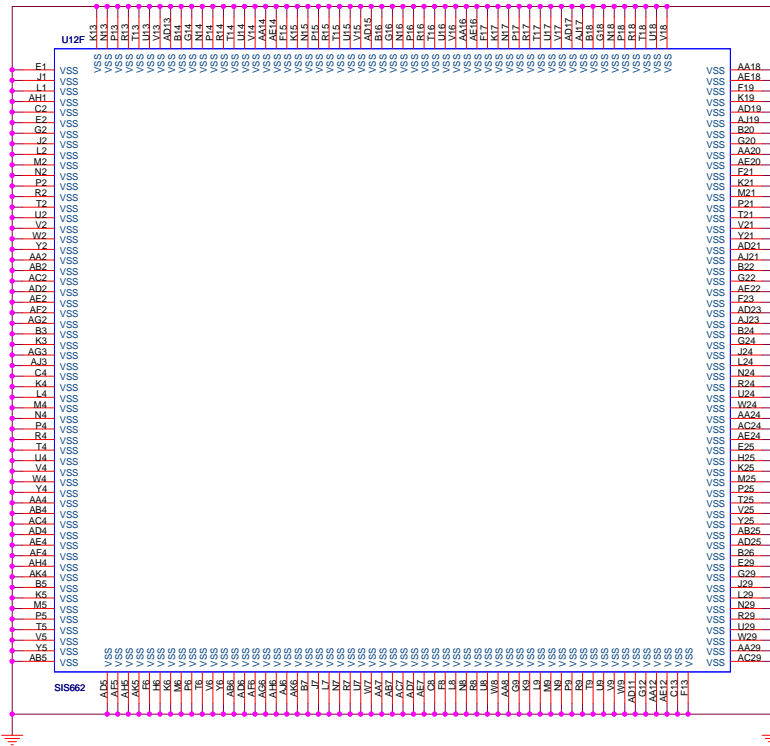
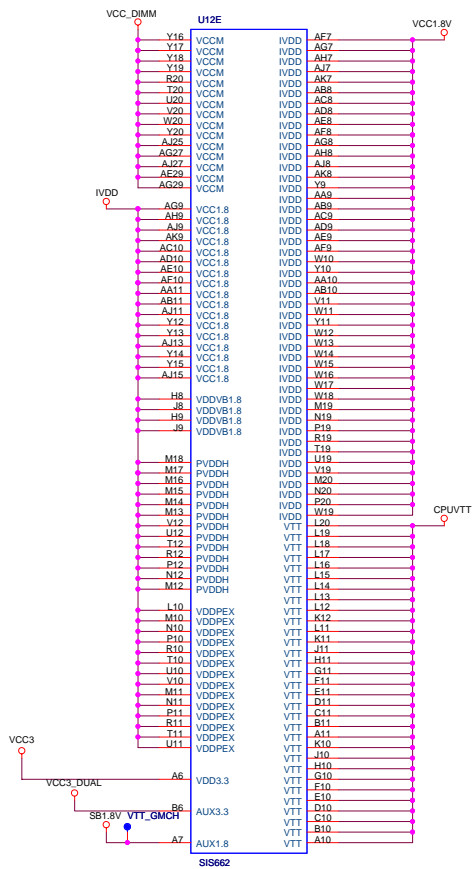
Title **662/1066T-M**

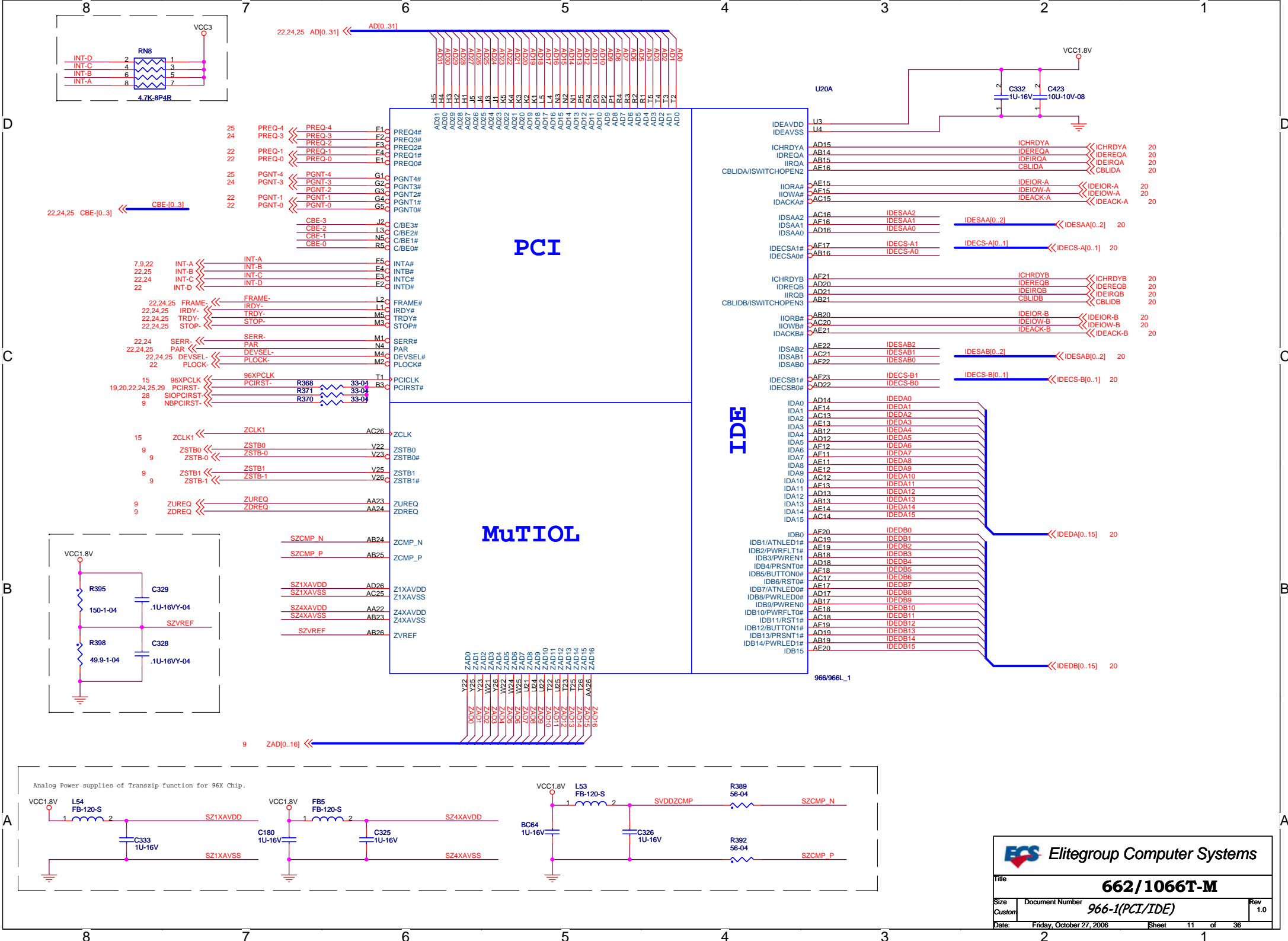
Size β Document Number **LGA755-3 (Power)** Rev 1.2

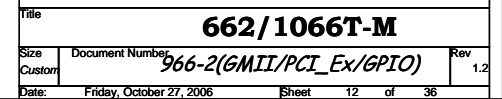
Date: Friday, October 27, 2006 Sheet 6 of 36

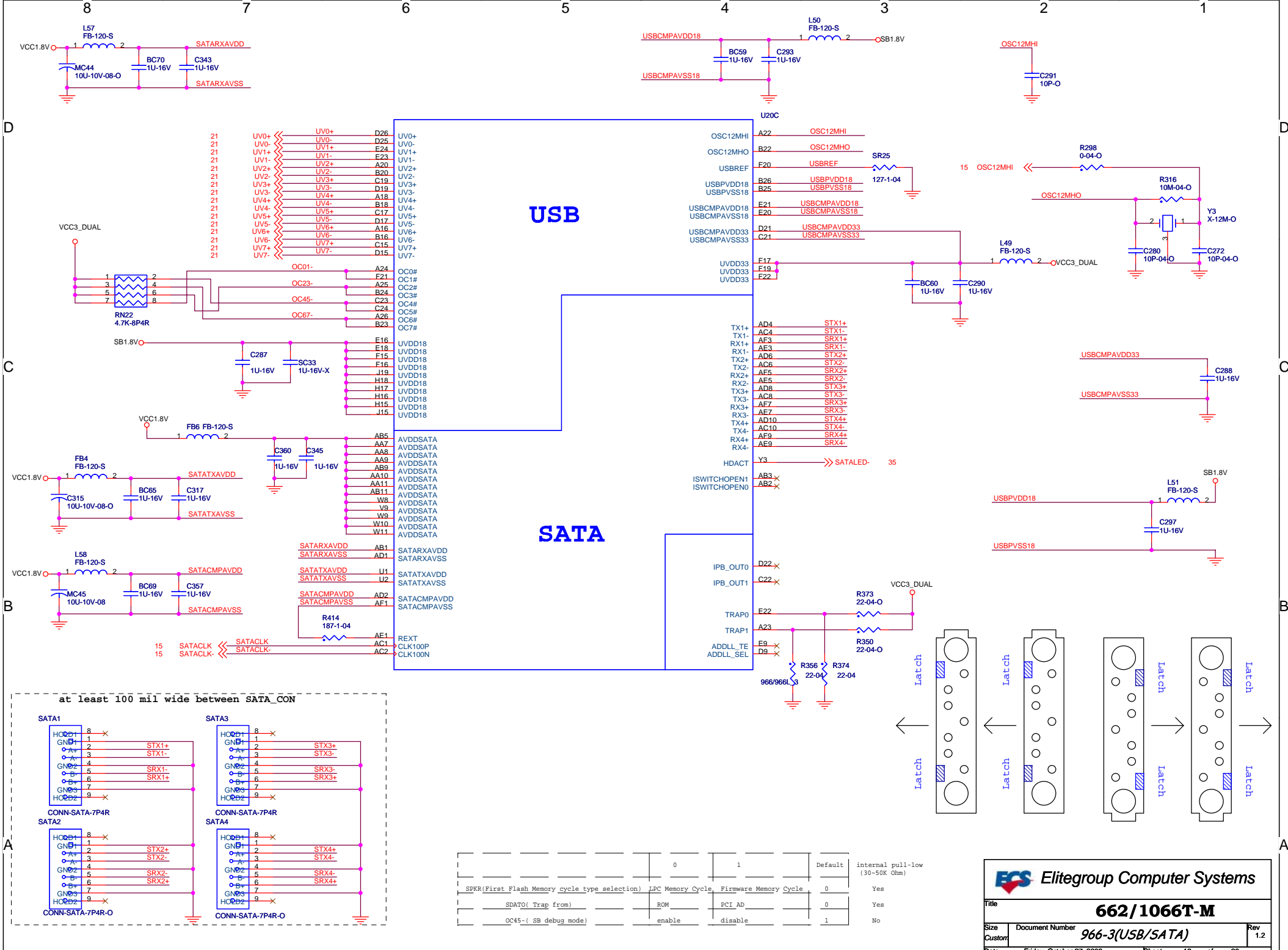








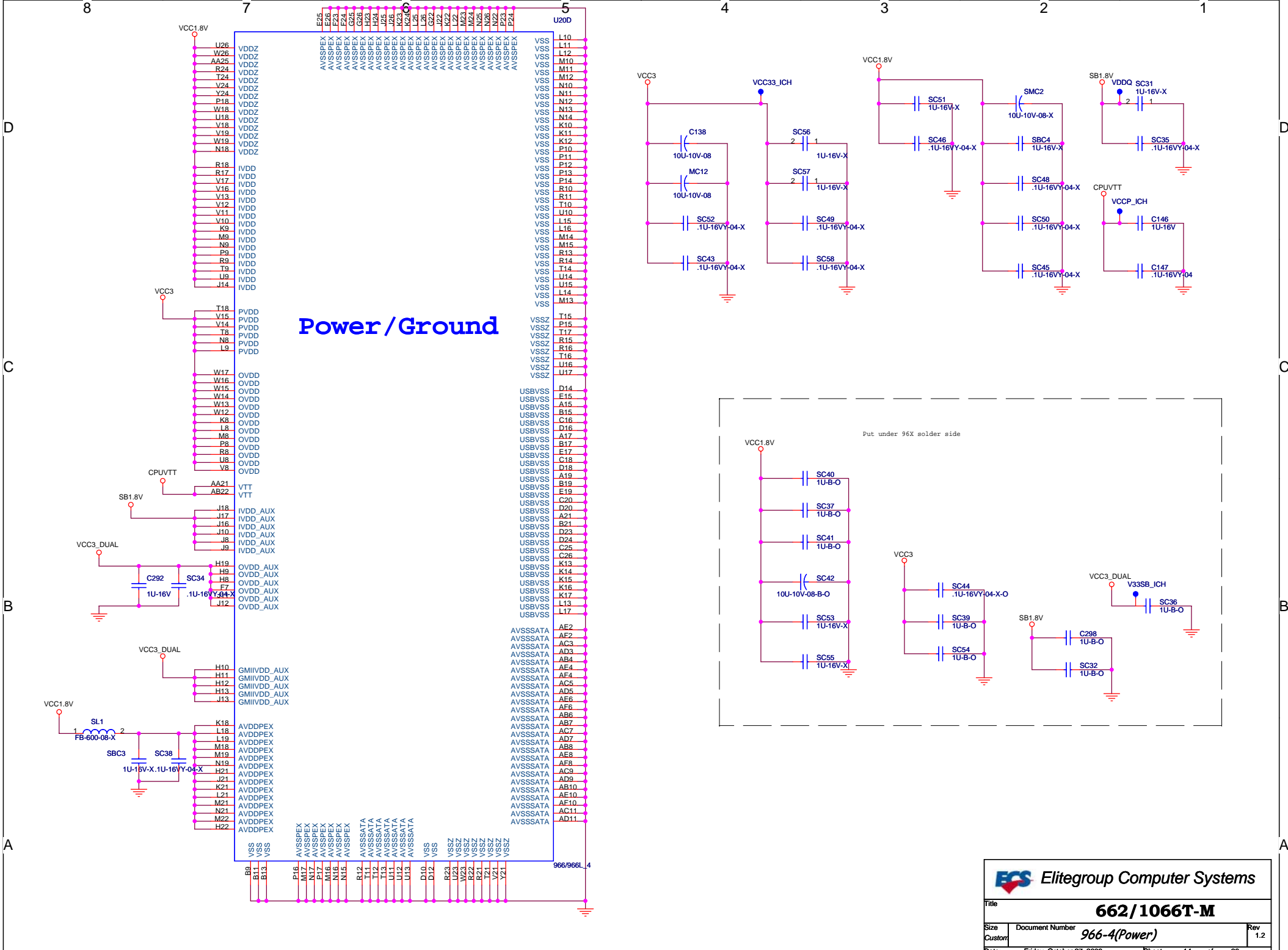




	0	1	Default	internal pull-low (30-50K Ohm)
SPKR(First Flash Memory cycle type selection)	LPC Memory Cycle	Firmware Memory Cycle	0	Yes
SDAT0(Trap from)	ROM	PCI AD	0	Yes
OC45-(SB debug mode)	enable	disable	1	No


Title
662/1066T-M

Size	Document Number	Rev
Custom	966-3(USB/SATA)	1.2
Date:	Friday, October 27, 2006	Sheet 13 of 36



Power / Ground

Put under 96X solder side

**Elitegroup Computer Systems**

Title			662/1066T-M
Size	Document Number	Rev	
Custom	966-4(Power)	1.2	
Date:	Friday, October 27, 2006	Sheet	14 of 36

Main Clock Generator

Damping Resistors
Place near to the
Clock Outputs

By-Pass Capacitors
Place near to the Clock Outputs

Follow ICS suggestion.

Frequency Selection

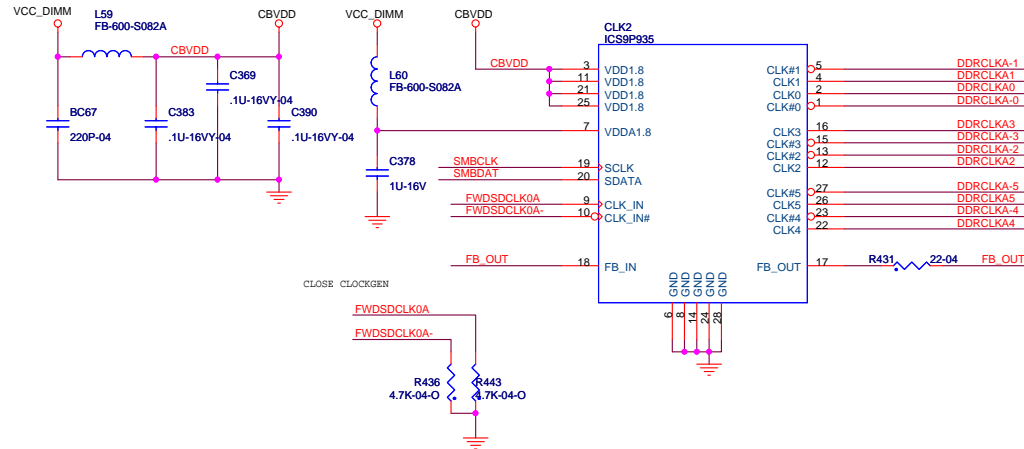
Clock Generator Table	FS4	FS3	FS2	FS1	FS0
Hardware Trapping	Low	Low	BSEL2	BSEL1	BSEL0
CPU=100 (BSEL[2:0]=101)	0	0	1	0	1
CPU=133 (BSEL[2:0]=001)	0	0	0	0	1
CPU=166 (BSEL[2:0]=011)	0	0	0	1	1
CPU=200 (BSEL[2:0]=010)	0	0	0	1	0
CPU=266 (BSEL[2:0]=000)	0	0	0	0	0
CPU=333 (BSEL[2:0]=100)	0	0	1	0	0
CPU=400 (BSEL[2:0]=110)	0	0	1	1	0

Modified R840, R841, and R842 from 1K to 4.7K, and
R843, R844, and R845 from 4.7K to 1K.

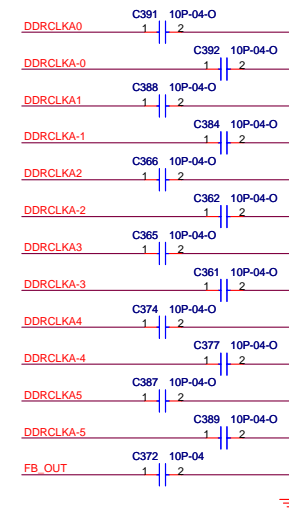
Clock Buffer (DDRII)

{ 5 OPTIONS }
 1: (ICS) ICS93716
 2: (Winbond)
 3: (ICWorks)
 4: (IMI)
 5: (AMI)

By-Pass Capacitors
 Place near to the Clock Buffer



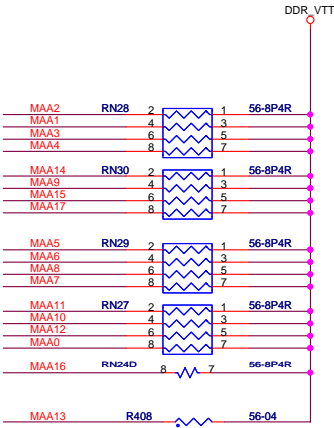
DDRCLKA[0..5] << DDRCLKA[0..5] 17
 DDRCLKA[0..5] << DDRCLKA[0..5] 17
 SMBCLK << SMBCLK 12,15,17,19,23,28,36
 SMBDAT << SMBDAT 12,15,17,19,23,28,36
 FWDSDCLK0A << FWDSDCLK0A 8
 FWDSDCLK0A- << FWDSDCLK0A- 8



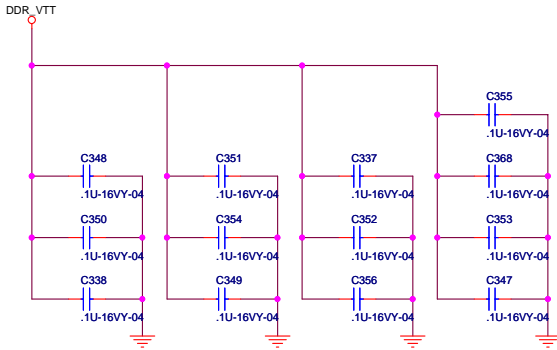
SSTL-2 Termination Resistors

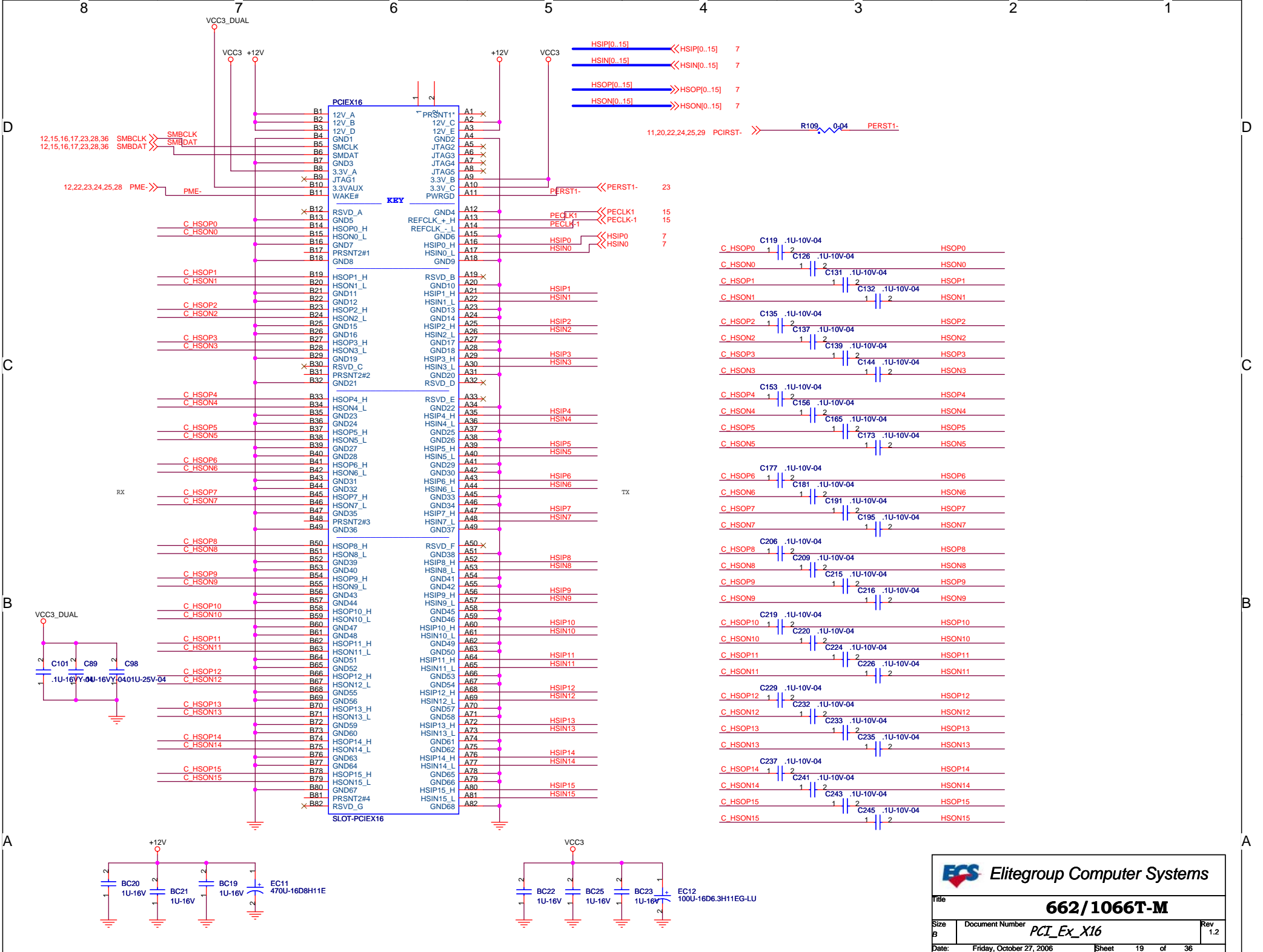
	DDR		DDR		Rtt
MD/DQM(/DQS)	LV-CMOS	DS	SSTL-2	DS	33
MA/Control	LV-CMOS	DS	SSTL-2	DS	33
CS	LV-CMOS	DS	SSTL-2	DS	47
CKE	DD 3.3V		DD 2.5V		

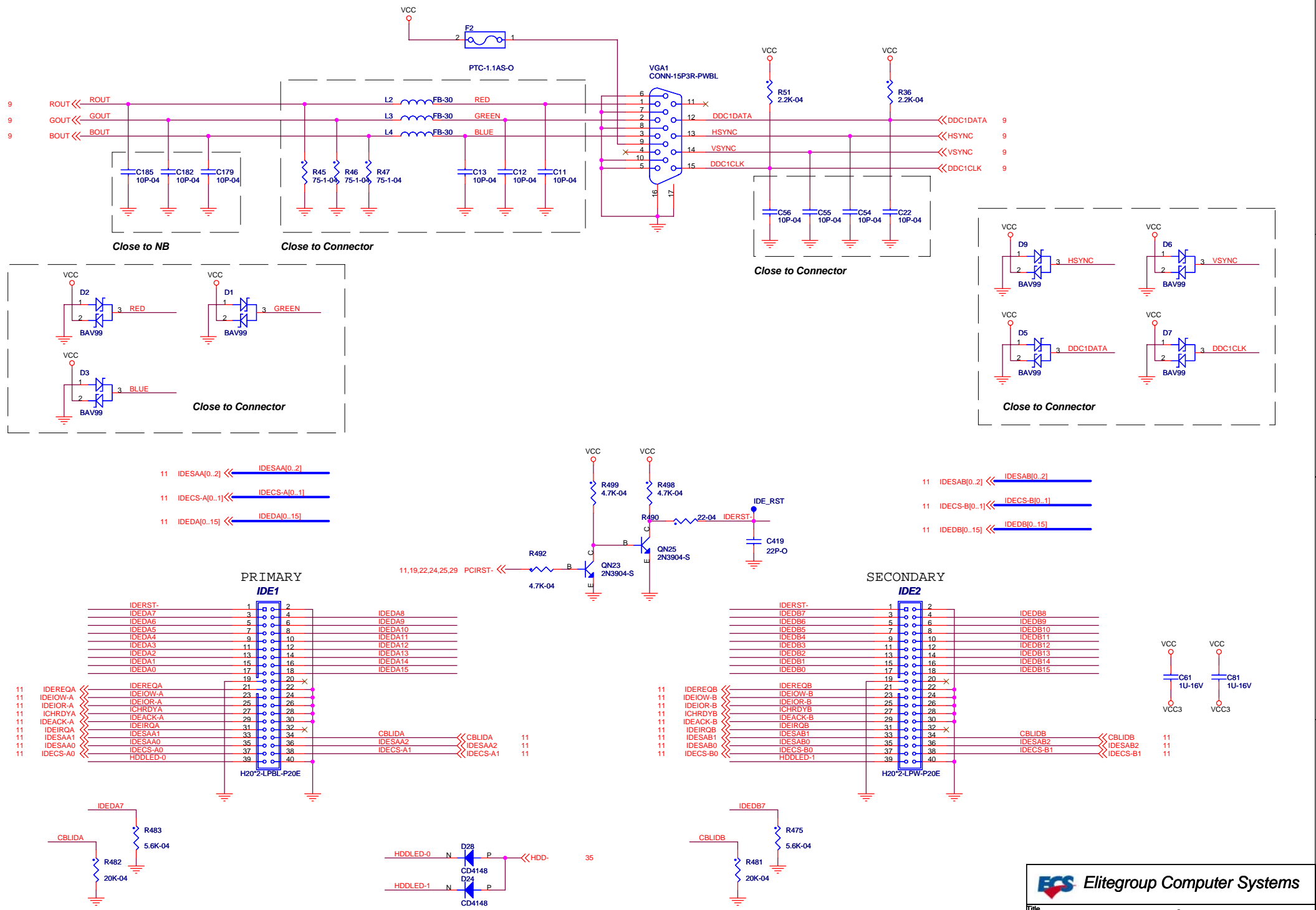
MAA[0..17] << MAA[0..17] 8,17

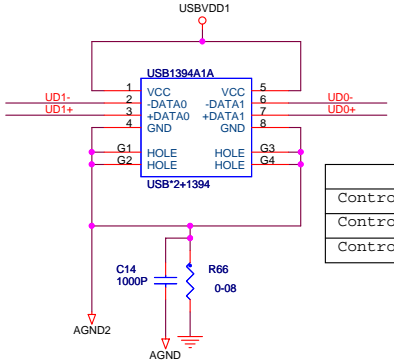
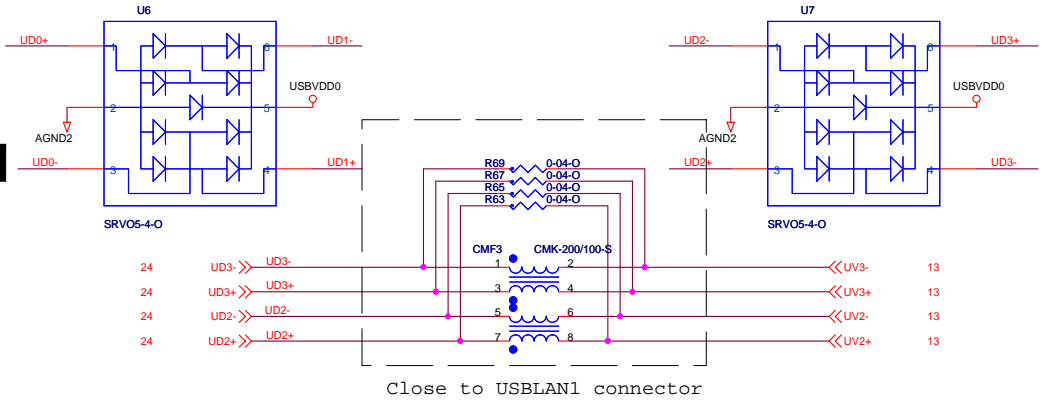
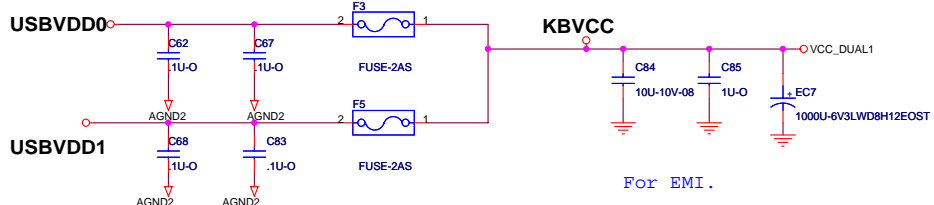
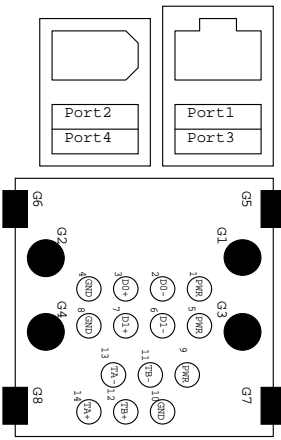


DECOUPLING CAPACITOR FOR SSTL-2 END TERMINATION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs

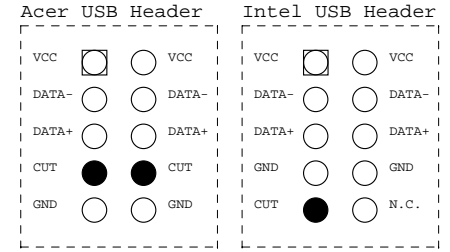
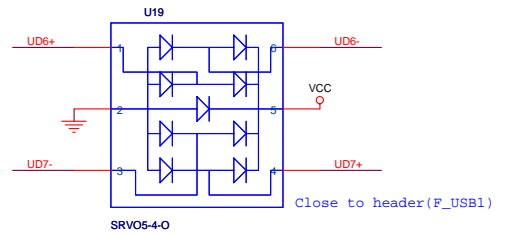
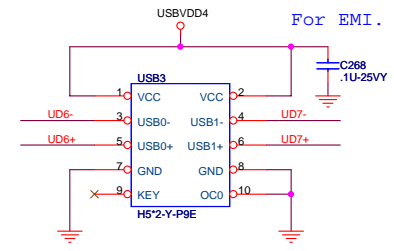
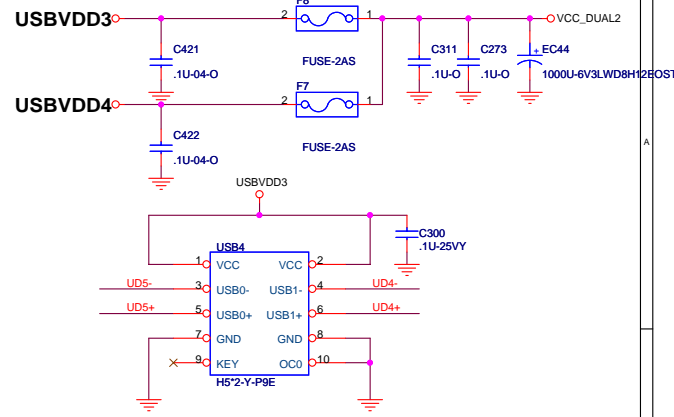
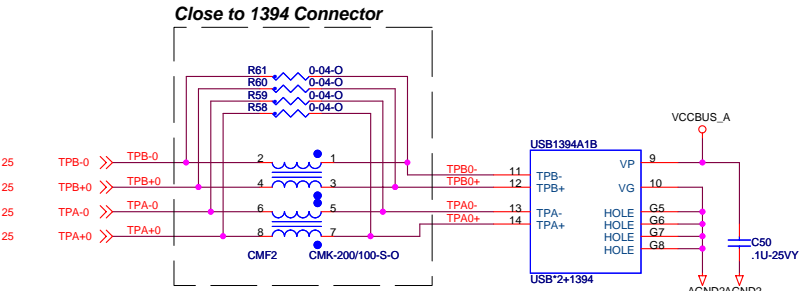
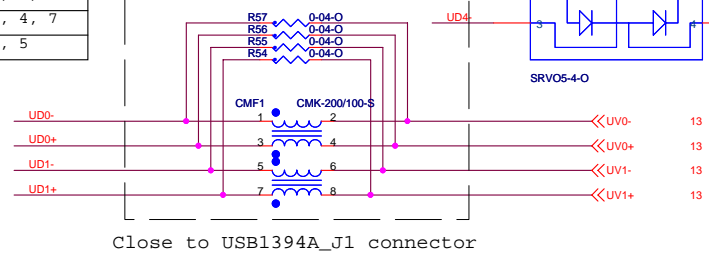






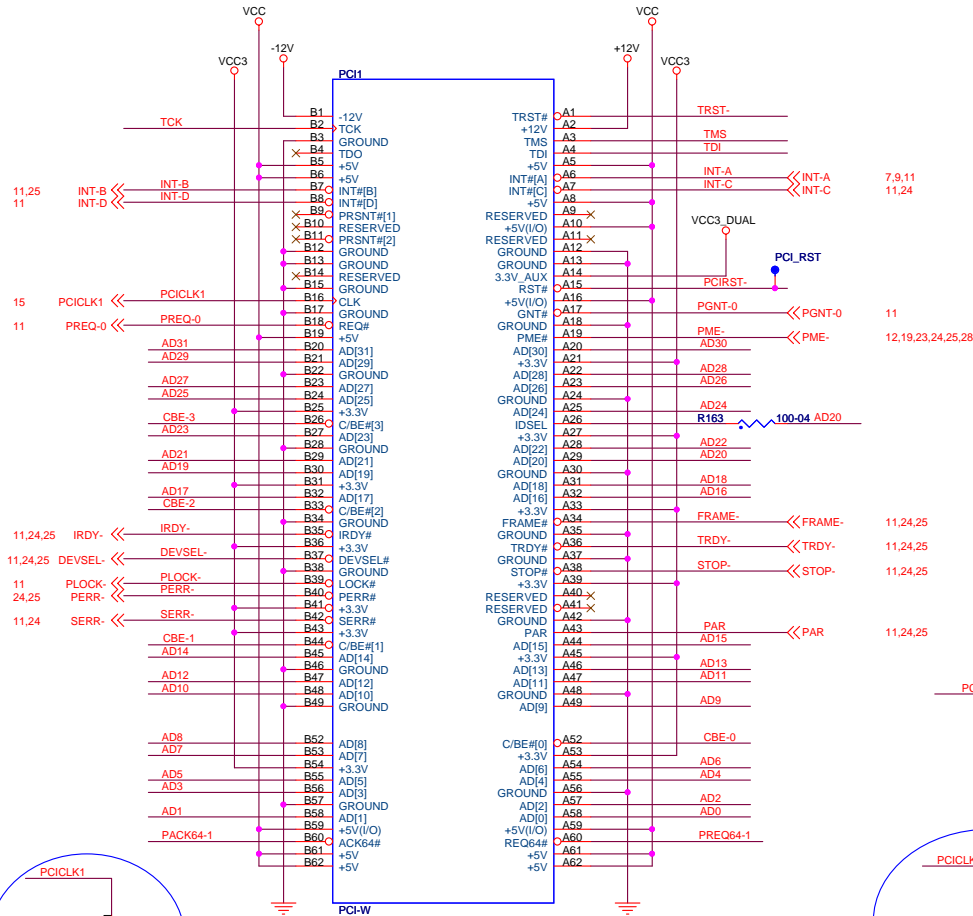


	USB port
Control 0	0, 3, 6
Control 1	1, 4, 7
Control 2	2, 5



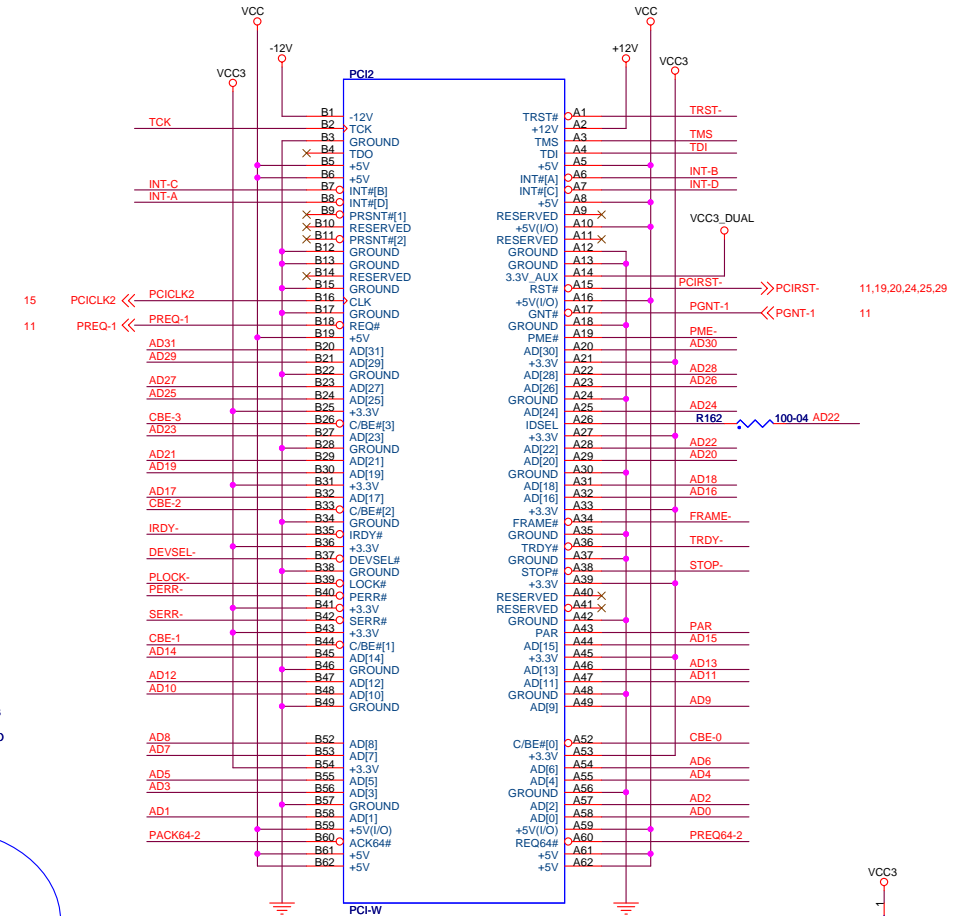
PCI Slot 1 & 2

11,24,25 CBE-[0..3] << CBE-[0..3]
11,24,25 AD[0..31] << AD[0..31]



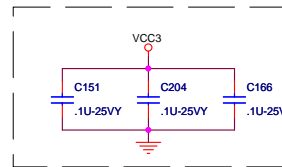
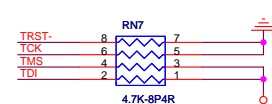
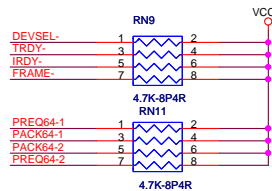
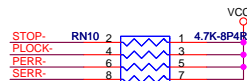
IDSEL=AD20
INT[A,B,C,D]
PCIx3=slot2
PCIEx1+PCIx2=slot1

Please place the cap close PCI Slot.

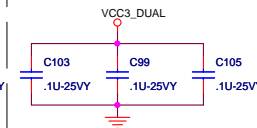


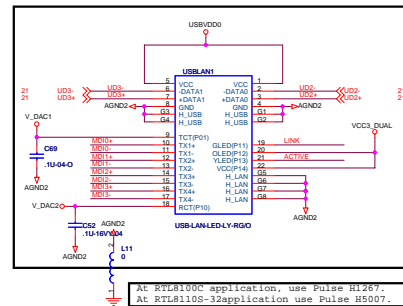
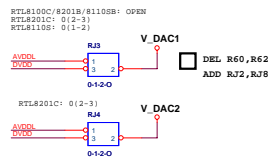
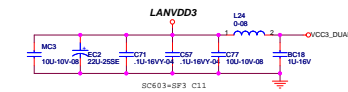
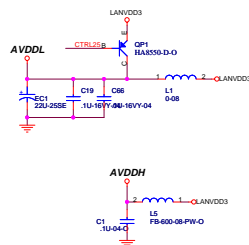
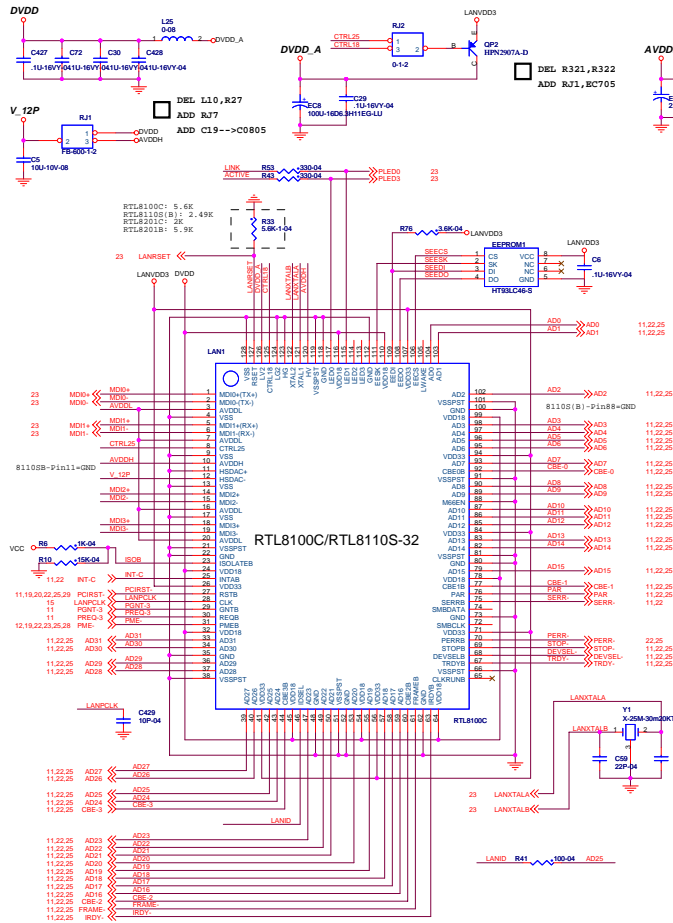
IDSEL=AD22
INT[B,C,D,A]
PCIx3=slot3
PCIEx1+PCIx2=slot2

Please place the cap close PCI Slot.



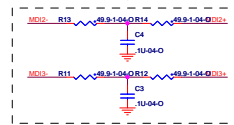
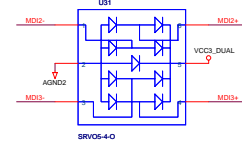
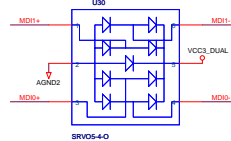
每個 PCI 插槽 pin A33
各放一顆



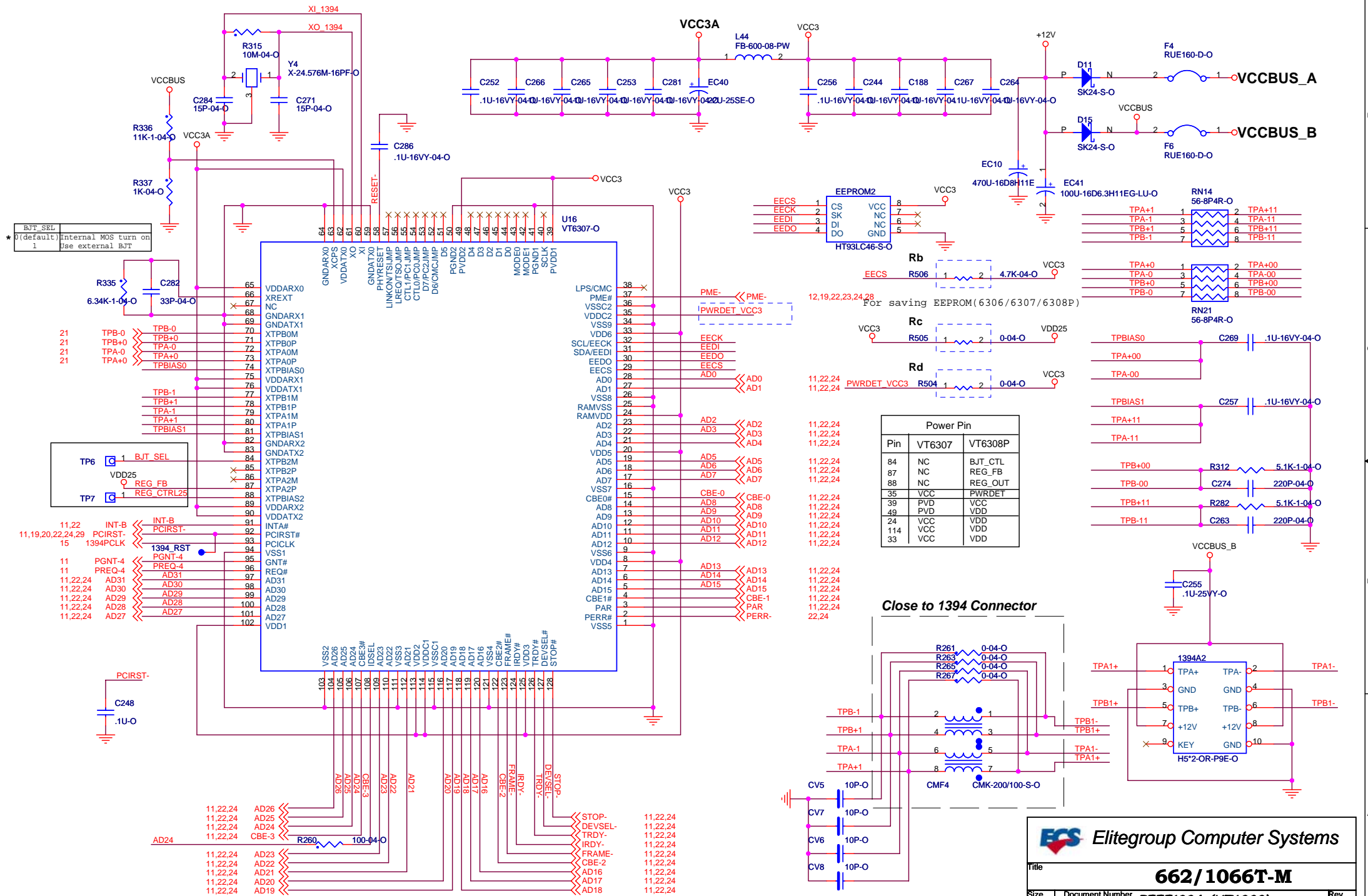


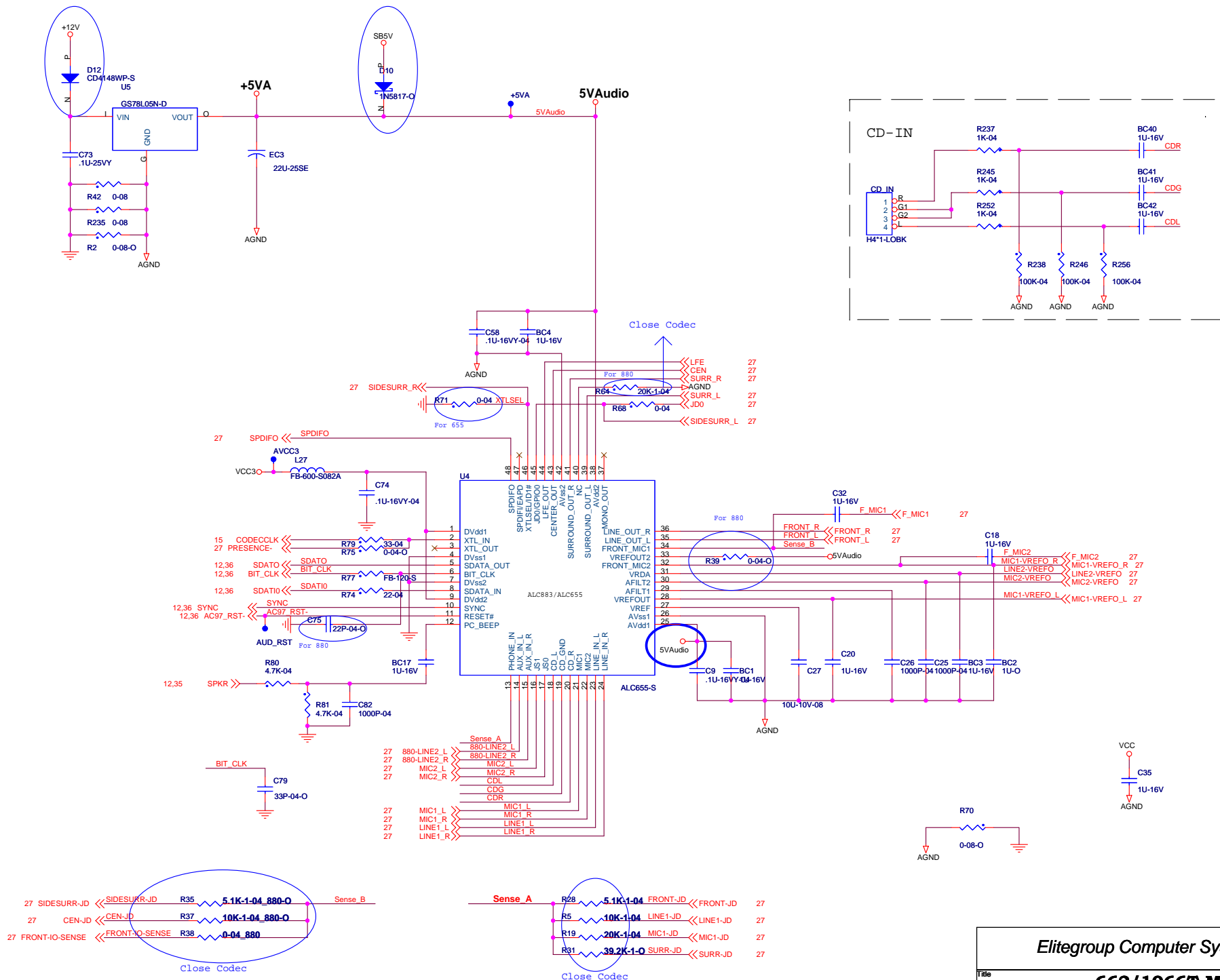
	8100C	8110S	8110SB
VDD3	3.3V	3.3V	3.3V
AVDDH	X	3.3V	3.3V
AVDDL	3.3V	2.5V	2.5V
DVDD_A	2.5V	1.8V	1.2V
DVDD	2.5V	1.8V	1.2V
V_L2P	2.5V	X	3.3V

At RTL8100C application,
remove R21, R28, R12, R14,
C18, C10, C52, C53, C54, and
change C51 value from 0.1uF
to .1uF.



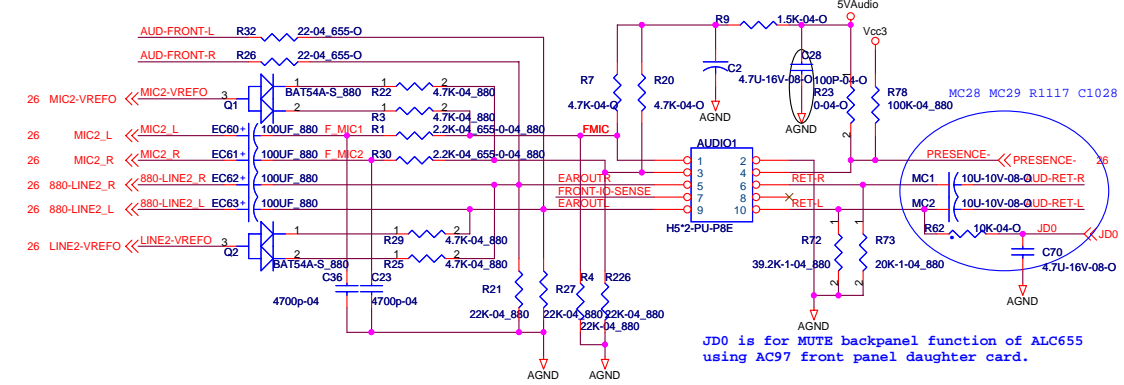
RTL8100C: OPEN
RTL8110S: Mounted



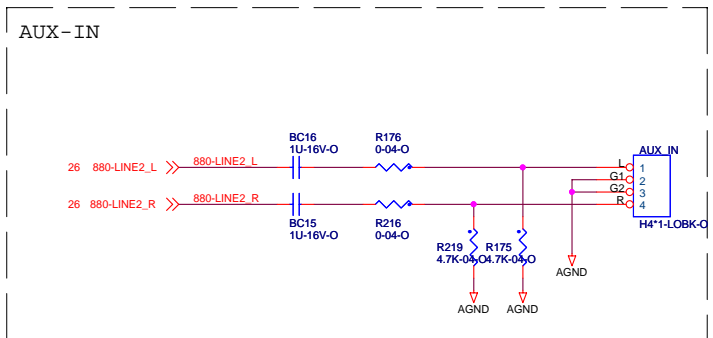
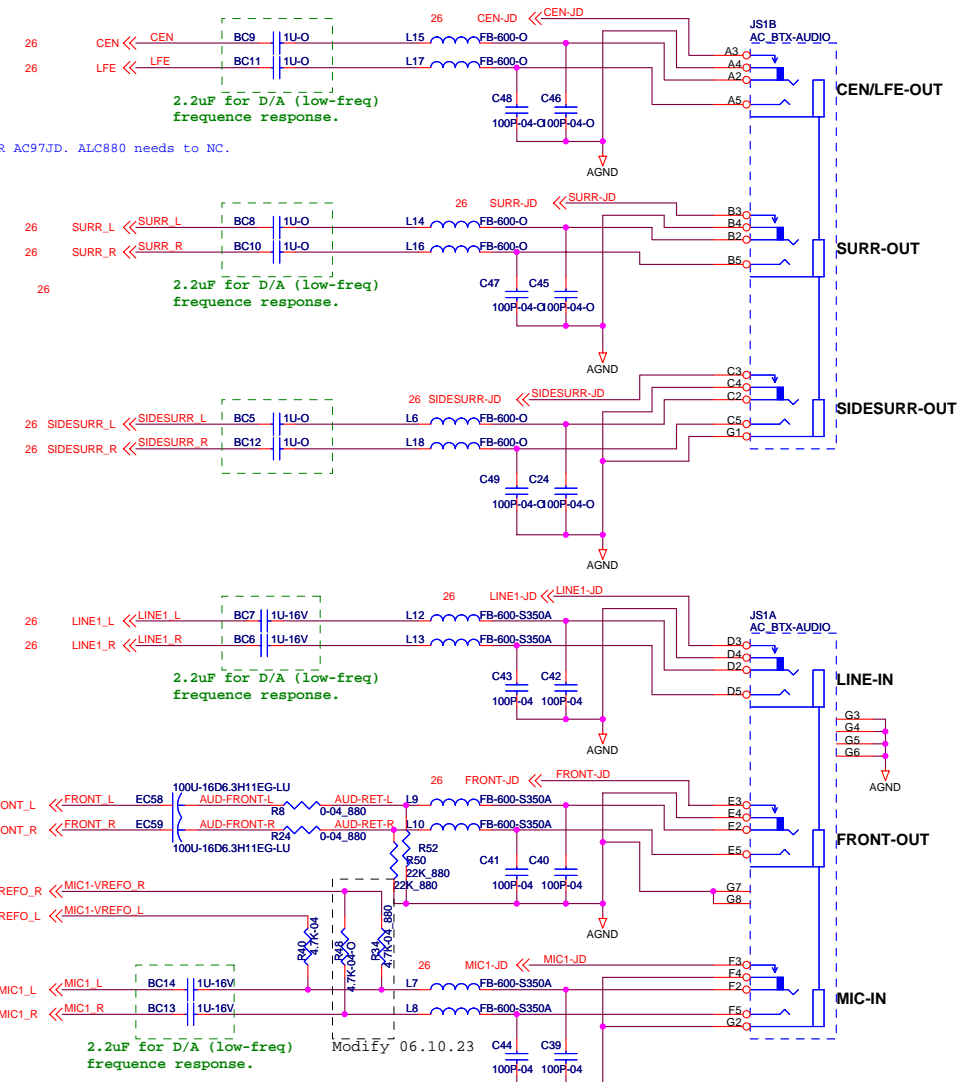
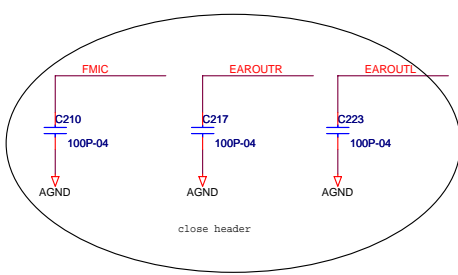
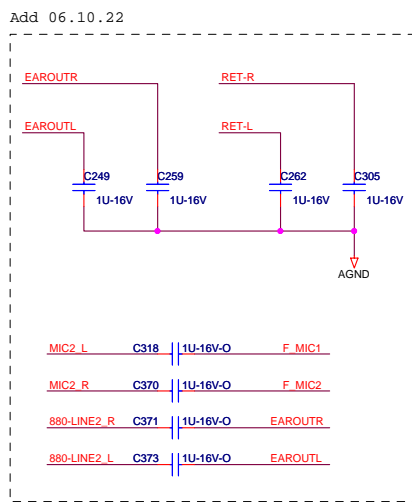
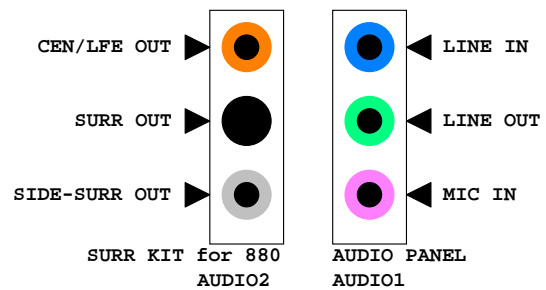


26 F_MIC1 << F_MIC1
 26 F_MIC2 << F_MIC2
 26 FRONT-IO-SENSE << FRONT-IO-SENSE

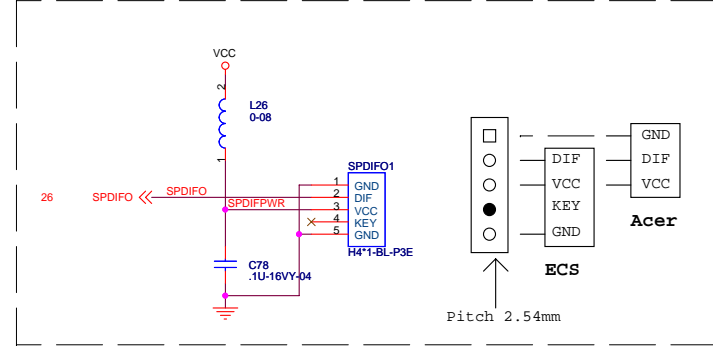
AC97/HDA FRONT HEADER

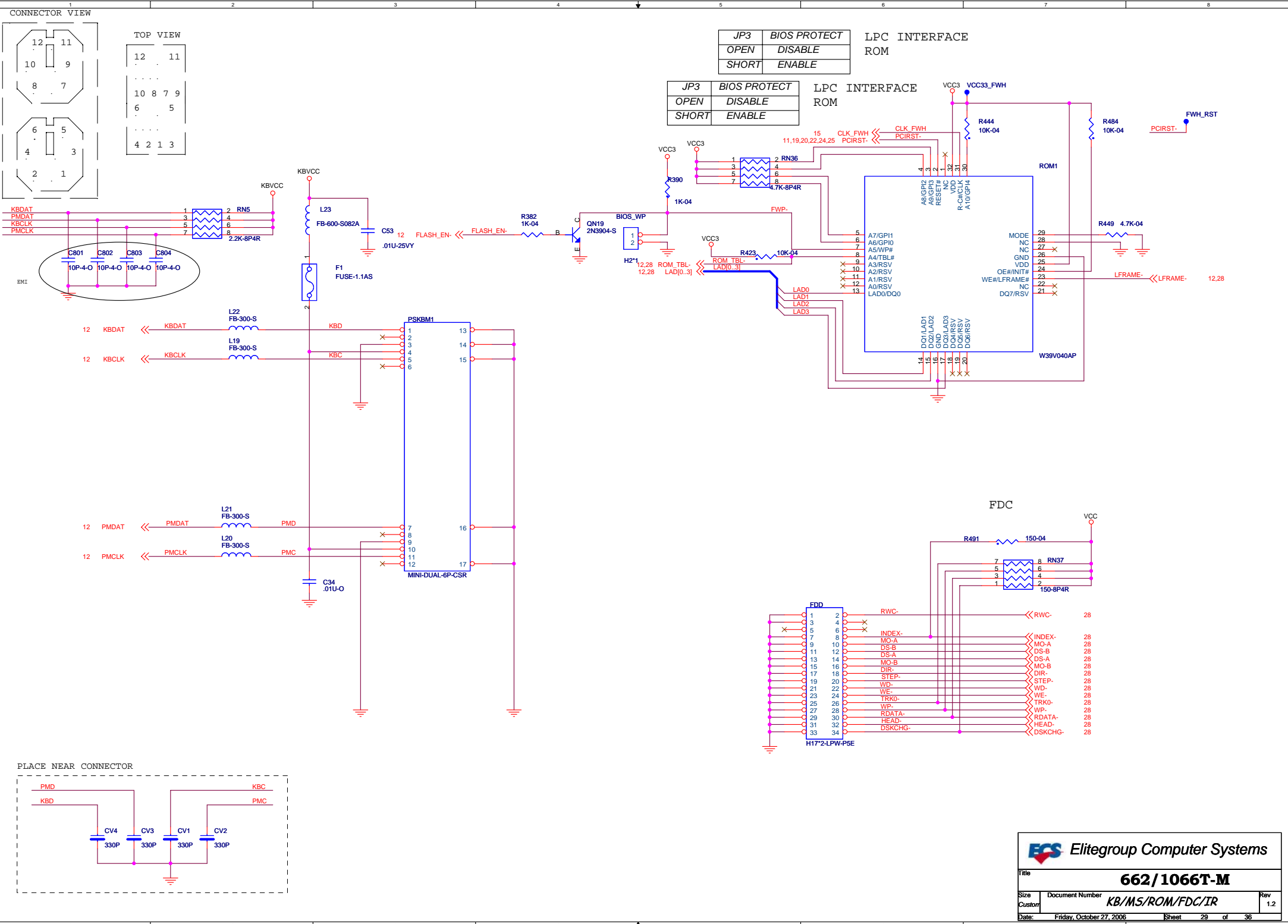


JD0 is for MUTE backpanel function of ALC655 using AC97 front panel daughter card.



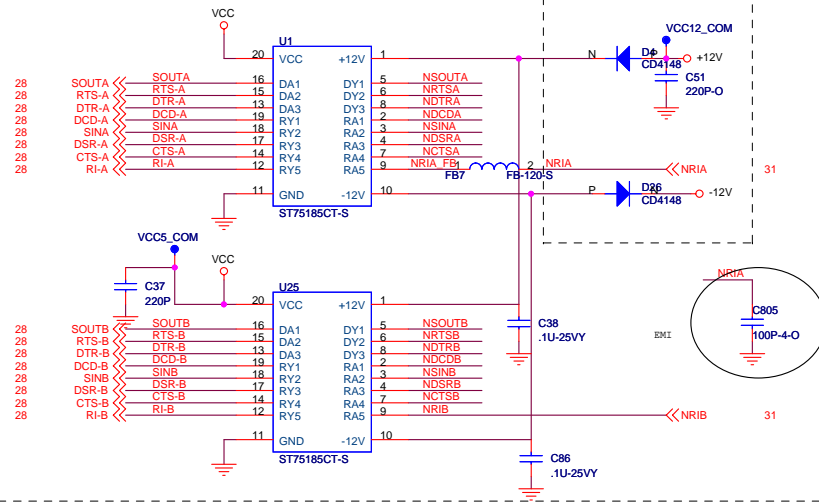
SPDIF-Out Pin Definition



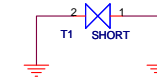
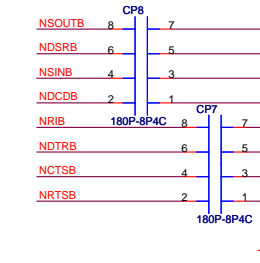
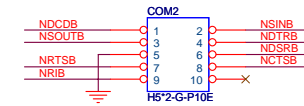
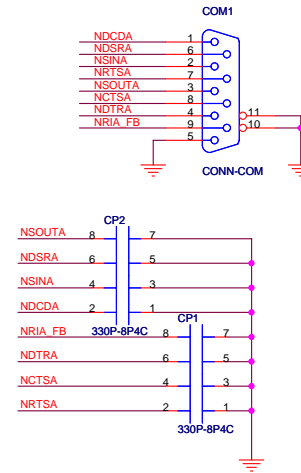


COM

close to IC

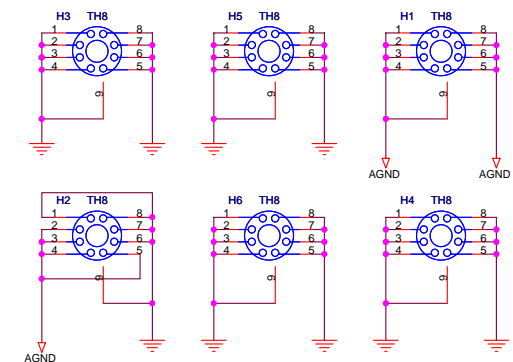
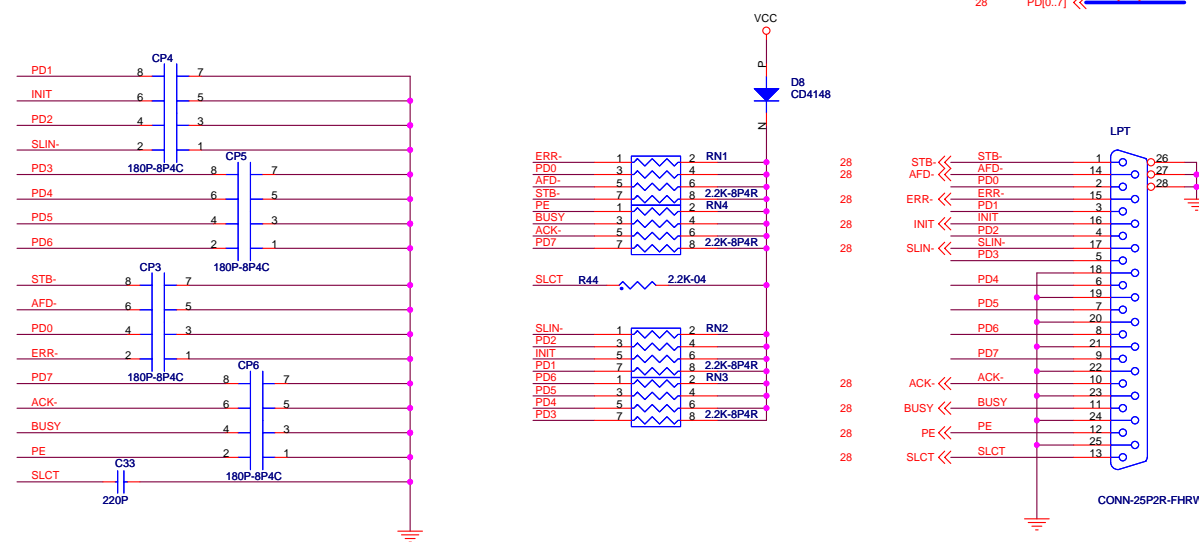


COM1 USE CONNECTOR



FIO的地

PRT



Elitegroup Computer Systems

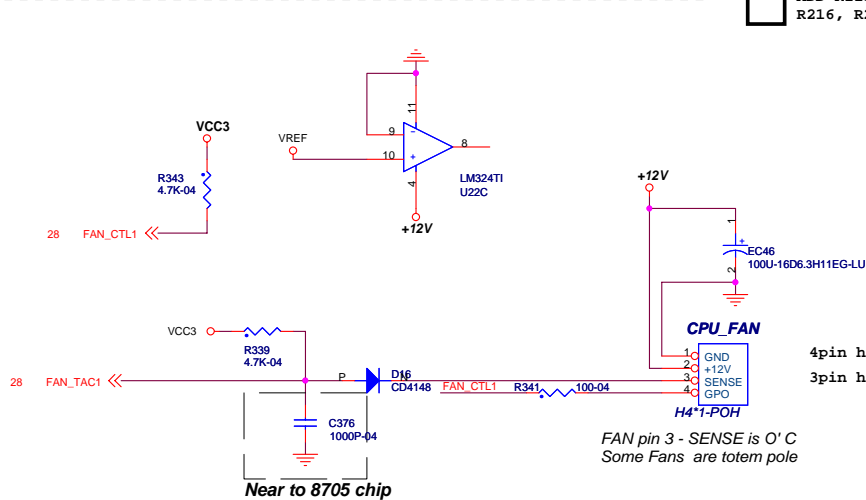
File: 662/1066T-M

Size: Custom Document Number: COM 1,2 / LPT

Date: Friday, October 27, 2006 Sheet 30 of 36

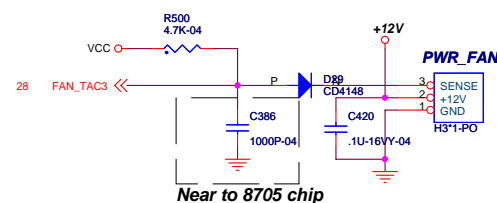
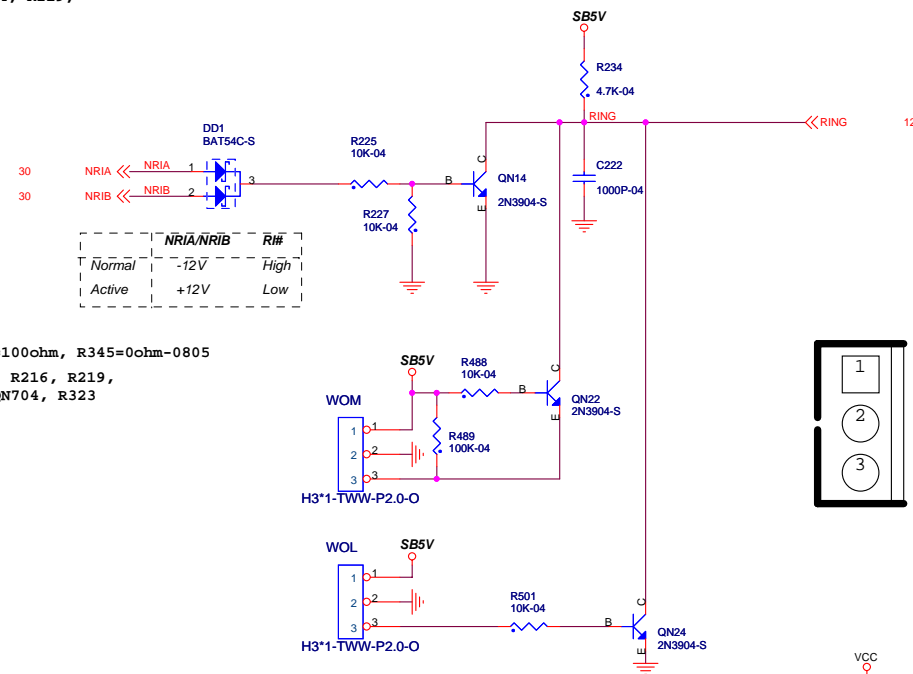
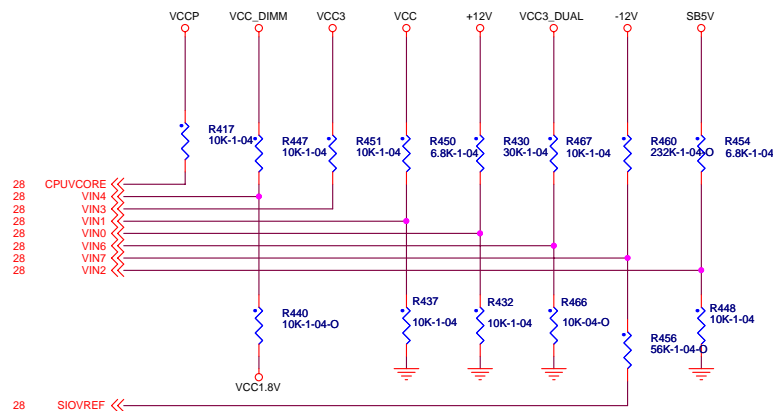
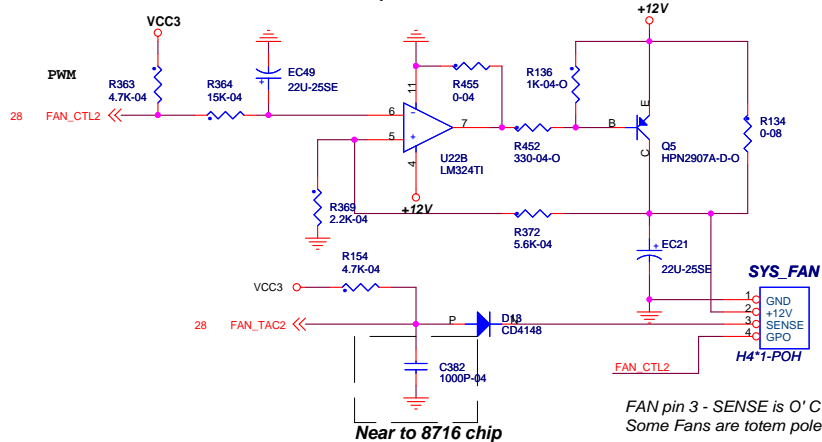
Power Signals : CPUFAN, CASEFAN, PWRFAN trace width should > 20 mil with current 200 mA .

ADD R223, EC46, R323, R324, R219,
R216, R225, Q5, QN704

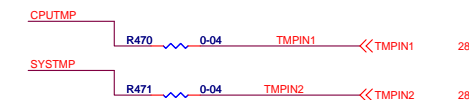
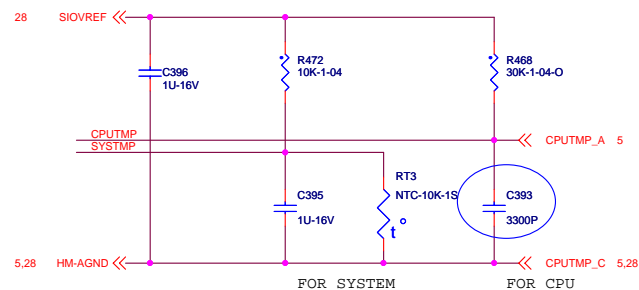


4pin header: QN17, R341=100ohm, R345=0ohm-0805

3pin header: R223, EC46, R216, R219,
Q5, R324, QN704, R323



Choosing method of measuring temperature by
either thermistor or diode



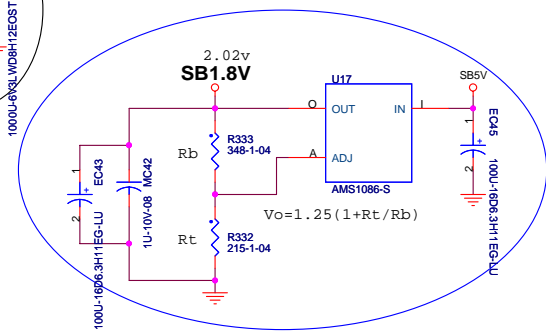
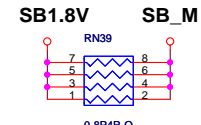
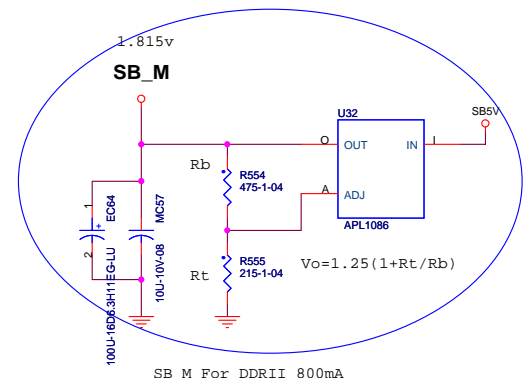
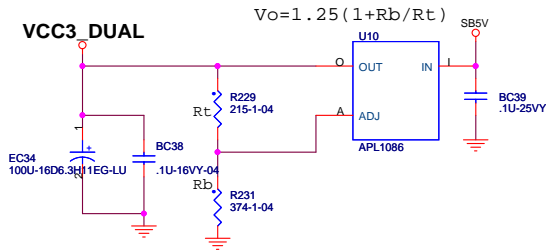
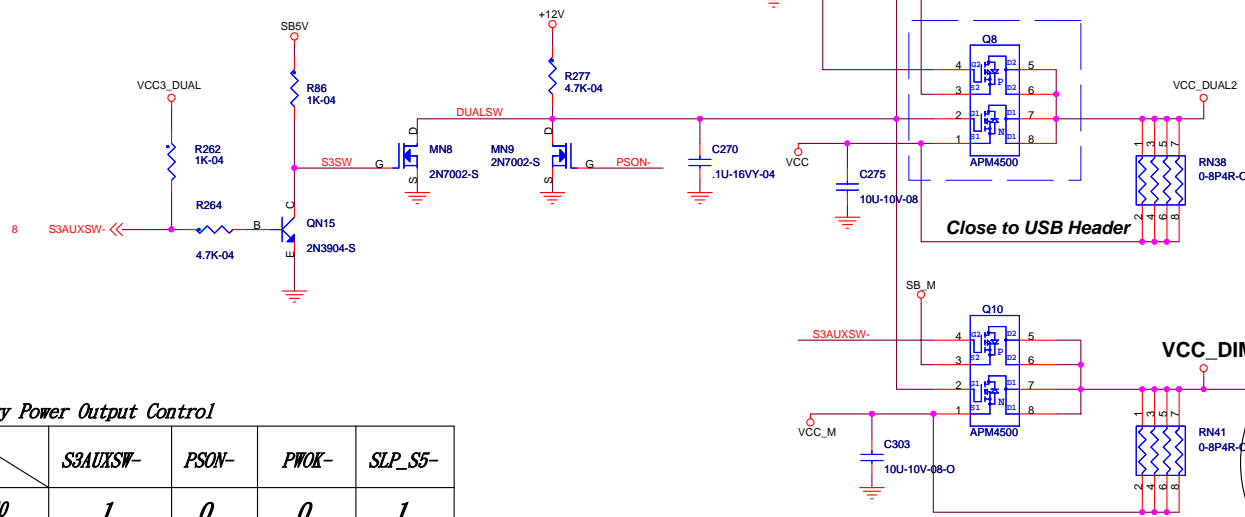
AUTO VOLTAGE SWITCH FOR ACPI STATE 3

1.IN S0,S1
THIS CIRCUIT PASSES THE NORMAL POWER

2.IN S3,S4,S5
THIS CIRCUIT PASSES THE STANDBY POWER

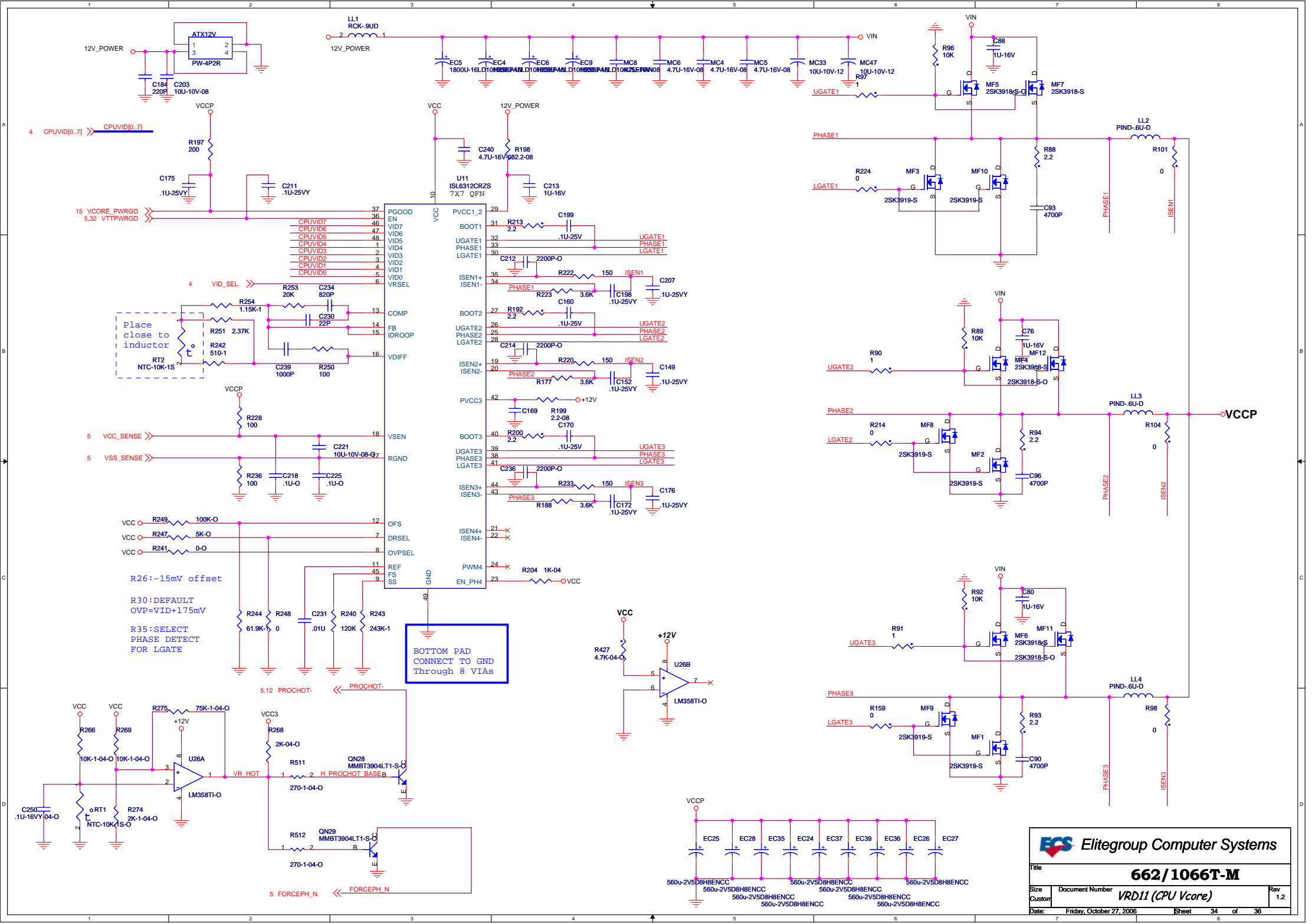
NOTE:
BECAUSE OF THE MAXIMUM CURRENT FROM
POWER SUPPLY IS ONLY ABOUT 750-1000mA
SO IF YOU WANT TO SUPPORT WAKE UP
FROM S3 BY USB, YOU MUST HAVE A POWER
SUPPLY WITH LARGER POWER. (ADDITIONAL
500mA PER USB PORT)

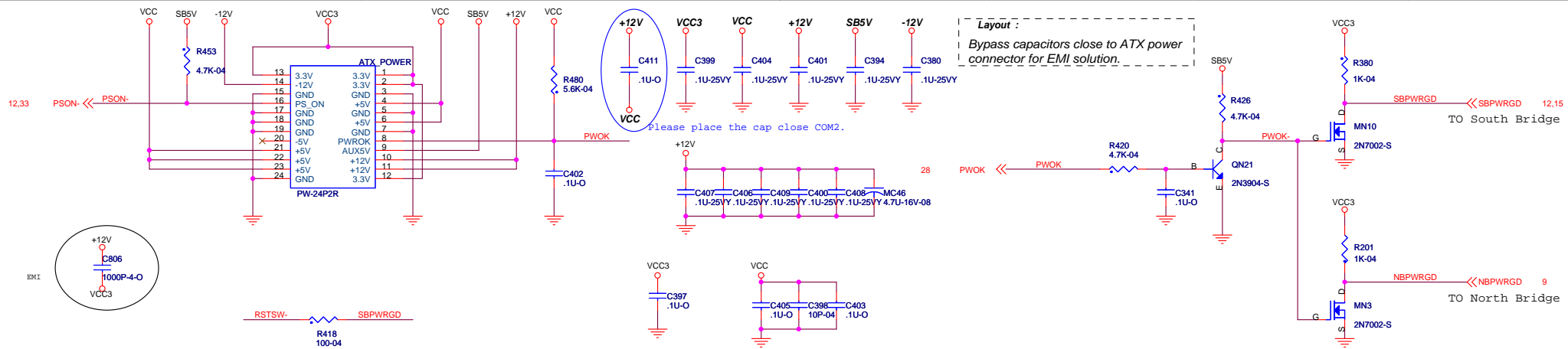
VCC3_DUAL & VCC5_DUAL



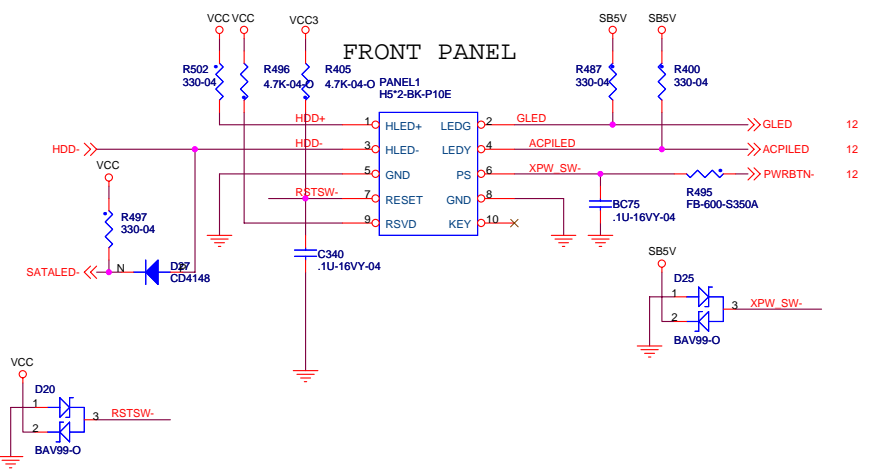
Memory Power Output Control

	S3AUXSW-	PSON-	PWOK-	SLP_S5-
S0	1	0	0	1
S1	1	0	0	1
S3	0	1	1	1
S4	1	1	1	0
S5	1	1	1	0

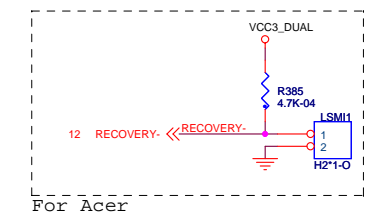
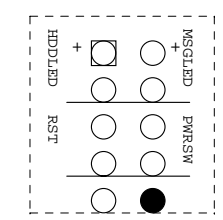




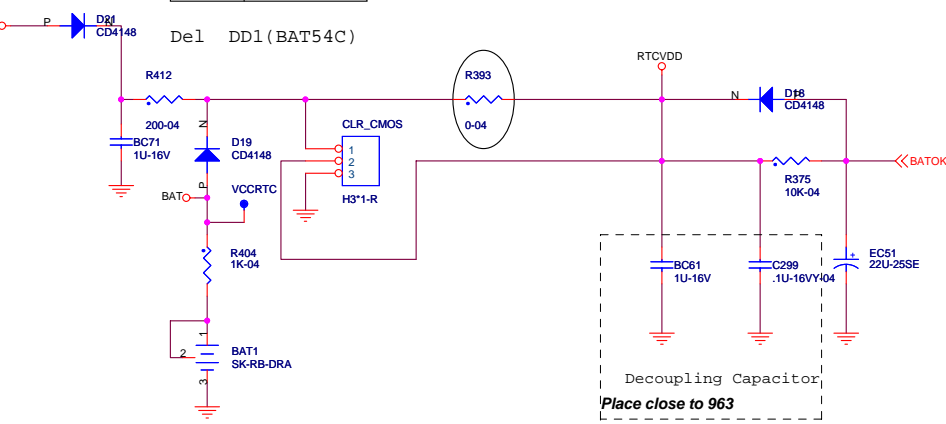
Hardware Reset Circuit



Intel Front Panel



JP1	CLEAR CMOS
1-2	NORMAL
2-3	CLEAR



NOTE!
 1.The RTCVDD is 3V
 2.Decoupling capacitor must be close to 635 RTCVDD pin.
 3.RTC circuit must strictly follow SiS's recommended design
 SiS is not responsible for RTC problems from foreign designs.

R1,R2,R3,R4 depend on the address selection.

ADD0	ADD1	ADDRESS
GND	GND	0x48
OPEN	GND	0x49
VCC	GND	0x4A
GND	OPEN	0x4B
OPEN	OPEN	0x4C
VCC	OPEN	0x4D
GND	VCC	0x4E
OPEN	VCC	0x4F
VCC	VCC	0x50

